TM 11-5840-271-30/10

DEPARTMENT OF THE ARMY TECHNICAL MANUAL

FIELD (THIRD ECHELON) MAINTENANCE MANUAL

PROCESSING CENTER, RADAR DATA OA-4333/MSQ-28B TRACKING COMPUTER TEST AND DIGITAL DATA DISPLAY FUNCTIONS THEORY AND TROUBLESHOOTING

HEADQUARTERS, DEPARTMENT OF THE ARMY

AUGUST 1963

TAGO 1003-7A—August

WARNING

DANGEROUS VOLTAGES EXIST IN THIS EQUIPMENT

Be careful when working on dc power supply circuits or on ac line connections.

DON'T TAKE CHANCES

EXTREMELY DANGEROUS VOLTAGES EXIST IN ALL CONSOLE UNITS

TECHNICAL MANUAL
No. 11-5840-271-30/10

HEADQUARTERS,
DEPARTMENT OF THE ARMY
WASHINGTON 25, D.C., *1 August 1963*

FIELD (THIRD ECHELON) MAINTENANCE MANUAL

PROCESSING CENTER, RADAR DATA OA-4333/MSQ-28B TRACKING COMPUTER TEST AND DIGITAL DATA DISPLAY FUNCTIONS, THEORY AND TROUBLESHOOTING

*This manual supersedes TM 11-5840-271-30/10, 3 December 1962.

All illustrations are located in back of manual.

CHAPTER 1
INTRODUCTION

Section I. GENERAL

1. Scope

a. Content. This manual contains field maintenance information for two functions described as the tracking computer test function and the digital data display function; both functions are part of the Radar Data Processing Center OA-4333/MSQ-28B Subsystem. Field maintenance information in this volume consists of theory of operation, troubleshooting, alignment and adjustment, and test procedures. Illustrations supplement the text and troubleshooting charts reference unit and card assemblies within the function. Refer to TM 11-5840-271-30/1 for a complete list of manuals covering this equipment.

b. Index of Publications. Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions, changes, or additional publications pertaining to your equipment. DA Pam 310-4 is an index of current technical manuals, technical bulletins, supply bulletins, lubrication orders, and modification work orders that are available through publications supply channels. Tle index lists the individual parts (-10, -20, -35P, etc) and the latest changes to and revisions of each equipment publication.

c. Reports of Maintenance and Unsatisfactory Equipment. Use equipment forms and records in accordance with instructions in TM 38-750.

d. Report of Damaged or Improper Shipment. Fill out and forward DD Form 6 (Report of Damaged or Improper Shipment) as prescribed in AR 700-58 (Army), NAVSANDA Publication 378 (Navy), and AFR 71-4 (Air Force).

e. Comments on Manual. Forward all comments on this publication direct to: Commanding Officer, U.S. Army Electronics Materiel Support Agency, ATTN: SELMS-MP, Fort Monmouth, N.J. (DA Form 1598 (Record of Comments on Publications), DA Form 2496 (Disposition Form), or letter may be used.)

2. General Information

a. Graphic symbols used on the illustrations are in accordance with those listed in MIL-STD-15A, Electrical and Electronic Symbols, and MIL-STD-17A, Mechanical Symbols.

b. Components mentioned frequently in this volume are usually referred to by common name as listed in TM 11-5840-271-30/1.

c. Assembly numbers used on drawings refer to the manufacturer's part numbers.

d. Equipment panel markings are capitalized in text and are blocked on illustrations.

e. Broken lines on illustrations represent mechanical connections, solid lines indicate electrical connections, and heavy solid lines enclose circuit groups within the function.

f. The use of this volume requires a basic knowledge of transistors as contained in TM 11-690, and digital fundamentals as contained in TM 11-5895-264-25.

g. A circuit description of each standard circuit (such as flip-flops and logic gates) is contained in TM 11-5895-264-25.

h. Definitions of unusual terms used in this volume are contained in TM 11-5840-271-30/1.

3. Schematic Diagrams

a. The unit schematic diagrams for this function are contained in TM 11-5840-271-30/19.

b. The card assembly schematic diagrams for this function are contained in TM 11-5840-271-30/20.

c. The unit schematic diagrams for the power supplies and power control panels are contained in TM 11-5840-273-30.

Section II. DESCRIPTION AND DATA

4. Purpose of Equipment

The tracking computer test and digital data display functions are specialized test equipments designed primarily to check operation of other functions contained in the RDPC subsystem, and they are also used extensively during troubleshooting procedures of the other functions. Specific purposes of the tracking computer test function and the digital data display function are described in paragraphs 4*a* and 4*b* respectively.

a. Tracking Computer Test Function. The tracking computer test function, which is referred to as the computer test function, provides a means for several computer test operations. Each of these operations is listed below:

(1) Checking tracking computer computation reliability during manual or automatic tracking modes without interruption of normal tracking computer operations.

(2) Detecting and localizing malfunctions in the tracking computer circuits during troubleshooting procedures.

(3) Detecting certain malfunctions of the ARDME circuits and informing the tracking computer and DT consoles of the ARDME data reliability according to the selected computer operating mode.

(4) Clearing portions of the local memory for test purposes.

(5) Generates a 16 digit binary word signal which can be used for troubleshooting of other RDPC functions.

b. Digital Data Display Function. The digital data display function provides a visual display of any binary word containing up to 16 digits, which is generated in the RDPC subsystem by any function receiving the same timing signals as the display function. The purposes of this display are listed below:

(1) To observe information entered on the drum, 501047, during normal operating procedures, which provides a rapid means of checking the reliability of the storage function and the functions entering information on the drum.

(2) To detect and localize malfunctions occurring in any digital circuit during troubleshooting procedures. Information to be displayed is received through the storage function or directly from the output of the circuit being checked.

5. Use of Equipment

a. Computer Test Function. The computer test function tests the tracking computer by providing the means to generate computer test problems, select computer circuit output signals to be displayed during computations, present test problems to the computer, and observe results of the computer test computations.

(1) Tracking computer test problems are generated by operating 16 switches on the tracking computer test function control panel which generate a 16 digit binary information word. Twenty-two different information words are generated for each test problem and each word is entered in a particular word slot on a special band of the drum 501047. The special band, which is used only to store test problem information, is called the manual entry band (test band). Each test problem information word entered on the test band is previously calculated to provide known test results. Test problems to be generated are listed in the tracking computer troubleshooting procedures (TM 11-5840-271-30/9).

(2) Tracking computer circuit output signals are selected for display by inserting the computer test function patch board test probe into the patch board test point which carries the output signals to be displayed. A major cycle (program step) at which the desired display occurs is also selected on the computer test function control panel.

(3) Tracking computer test problems are presented to the tracking computer by pressing a start computation push button on the computer test set control panel; however, tracking computer computations do not start immediately. First, the tracking computer function and the ARDME function read out the test problem information contained on the test band and transfer the information serially, one information word during each drum revolution, to a special sector on the drum. The special

sector is one word slot in each of the 44 tracking computer computation bands, and is used to store only the computer test information. Sector No. 1 is the special test sector. The last word of the 22 information words read from the test band is a major cycle constant which starts the tracking computer program cycle, and the tracking computer continues computations using the test problem information for each of the 68 program steps.

(4) At the preselected major cycle, the selected tracking computer circuit output signal is entered into the computer test function display register and a computer test result is displayed. Displayed test results are then compared with previously calculated results, which are given in the tracking computer troubleshooting procedures, to determine if any malfunctions exist in the circuit being checked. Each time a different circuit output is selected to be displayed or a different major cycle is selected for a display to occur, the tracking computer program cycle is repeated. The tracking computer test function general theory and detailed functional theory are described in chapter 2.

b. Digital Data Display Function. The digital data display function is used to display a binary word containing up to 16 digits. First, a binary signal to be displayed is selected, display conditions are selected which will provide a desired one word display from the selected signal, and the display operation is started to provide a one word display of the selected binary signal.

(1) Binary signals to be displayed are selected from either the digital data display function patch board or directly from the output of the circuit being checked. Each signal selected from the digital data display function patch board is received from a band on the drum. The output signal from any digital circuit in the RDPC subsystem may be selected for display by connecting the patch board test probe to the desired output signal, providing the circuit being checked receives the same timing signals as the digital data display function.

(2) Display conditions are selected depending upon the signal selected for display. When the signal to be displayed is selected from the patch board, display conditions providing a one word display of the selected signal are obtained by selecting a drum sector that contains the desired word. Display conditions for signals taken directly from digital circuits are obtained by connecting all the display conditions, which provides a one word binary display, into a special gate on the digital data display function control panel. Additional timing is provided in either case, if desired, by selecting a particular program step for the display to occur.

(3) The display operation is started when a start display push button is pressed. The selected binary word then enters the display register and is displayed when the selected display conditions occur. The digital data display function general theory and detailed functional theory are described in chapter 3.

CHAPTER 2
COMPUTER TEST FUNCTION, THEORY OF OPERATION

Section I. GENERAL THEORY

6. General

This section contains general information concerned with operation of the computer test function. The physical location of the computer test function units (group 48) and the unit common names are contained in paragraph 7. Paragraph 8 lists all switches and indicators contained in the computer test function. The remaining paragraphs briefly describe the operations of the computer test function.

7. Description

(fig. 1)

The computer test function (group 48) consists of portions of two units of the RDPC subsystem. The following chart lists the unit number, common name, location, and content of both units.

Manufacturer's part No.	Common name	Group	Reference designation	Level	Content
501051	Computer test set and display control.	30, 48	44	A and C	Level A contains the computer test function control panel and level C contains most of the control flip-flops.
501056	Display test set and computer test control.	30, 48	49	C	Contains the display register flip-flops, major cycle number compare flip-flop, and the slot coincidence flip-flop

8. Switches and Indicators

The computer test control panel on the 501051 unit contains all of the switches and indicators used during tracking computer tests except the MEMORY CLEAR pushbutton. The MEMORY CLEAR pushbutton is mounted on the front panel of the 501051 unit. In addition to the switches and indicators, 102 test points are also mounted on the control panel. A list of these test points and the signals which are applied to them is provided in section II, detailed functional theory. Paragraph 8*a* lists all computer test functions switches and paragraph 8*b* lists all indicators. The 501051 unit drawer must be pulled out to provide access to the control panel.

a. The following chart lists all computer test function switches and the numerical designation and uses of each switch.

Switch	Designation	Use
AUTO MODE OPERATIVE—INOPERATIVE.	S28	Prevents the tracking computer from operating in automatic mode when set in the INOPERATIVE position if the MAN MODE switch is in OPERATIVE position.

Switch	Designation	Use
ENTER INFO	S1	Provides the signal necessary to enter an information word on the manual entry band.
INFORMATION INPUT P0–P15.	S2 through S17	These 16 switches are used to generate a binary information test word which is entered on the manual entry band.
INFO SELECTOR TEST-PATCH.	S20	Selects either the manual entry band information or test results information to be displayed by the display register.
MAN MODE OPERATIVE—INOPERATIVE.	S27	Disables AUTO MODE switch so that only manual mode operation is possible when set in INOPERATIVE position.
MAJOR CYCLE SEL TENS.	S33	Selects the tens portion of the major cycle at which predetermined test result information occurs.
MAJOR CYCLE SEL UNITS.	S32	Selects the unit portion of the major cycle at which predetermined test results information occurs.
MEMORY CLEAR	S30	Clears local memory action bands 1 through 6 and major cycle tens and minor cycle band.
ONCE ONLY—EVERY DREV.	S24	Causes display to be inhibited at the selected major cycle or allows display to change configuration every drev.
PATCH BOARD TEST PROBE.	S25	Selects test results information from the patch board to be routed to the display register.
SLOT SEL LSD	S18	Selects the LSD–3rd LSD of the slot counter for manual entry band slot coincidence.
SLOT SEL MSD	S19	Selects the 4th LSD, MSD of the slot counter for manual entry band slot coincidence.
START COMPUTATION.	S26	Causes transfer of test information from manual entry band to test sector bands of drum memory.

b. The following chart lists all computer test function indicators and the designation and use of each indicator.

Indicator	Designation	Use
AUTO MODE	DS19	−26.5-volt lamp glows when both the MAN MODE and AUTO MODE switches are in the OPERATIVE position.
DISPLAY REGISTER	DS1 through DS16	These 16 six-volt lamps glow to indicate the binary word contained in the display register flip-flops.
MAN MODE	DS18	−26.5 volt lamp glows when the MAN MODE switch is in the OPERATIVE position.
REJECT ARDME DATA.	DS17	28-volt lamp glows to indicate an ARDME malfunction.

9. Computer Test Data Entry

(fig. 2)

Computer test data entry is the operation required to initiate a new tracking computer test problem and enter the initiated data on the manual entry band which is reserved for computer test data. The manual entry band is referred to as the test band. When initiating a computer test problem, a test band slot is selected, an information word generated, and then the data entry operation performed to enter each of the required 22 information words one at a time on the test band. The storage function test band is divided into 31-word slots which store the test data necessary to initiate a tracking computer problem. Each computer test requires that 22 information words be generated and each information word entered into a preselected test band word slot. Test band word slots are assigned to specific computer test information and, although the actual information word may change for each test problem, use of the information is the same for all computer tests. Information words required to initiate any particular computer test problem and the test band slot into which each information word is entered is determined by following the tracking computer troubleshooting procedures contained in TM 11-5840-271-30/9.

a. Test Band Slot Selection. Test band slot selection is provided by slot selector switches on the computer test control panel of the 501051 unit. SLOT SEL MSD switch S19 selects the test band slot tens count from 0 through 3 while SLOT SEL LSD switch S18 selects the test band slot unit count from 0 through 7. Combined operation of both switches allows any number between 0 and 37 in the octal numbering system to be selected. The slot selector switches are numbered in the octal numbering system to provide operating convenience during computer tests. Test band slot counts are generated by a test band slot counter and are applied to the contacts of the slot selector switches S18 and S19. Output signals from the switches represent the configuration of the test band slot counter, and are routed from the slot selector switches to a slot coincidence flip-flop. The slot coincidence flip-flop is set true when the output signals from S18 and S19 are true and this occurs only when the test band slot counter configuration is the same as the selected test band slot. When set true, the slot coincidence flip-flop remains true for one word time and then goes false until the selected slot count reoccurs. Output signals from the slot coincidence flip-flop are routed to a test band write flip-flop where the slot coincidence signals provide the timing necessary to enter an information word into a predetermined test band slot.

b. Input Information Selection. Input information selection is provided by 16 INFORMATION INPUT P0–P15 switches S2–S17 on the computer test control panel. Each of the 16 switches represents one digit of a 16 digit binary work. The digit represented is either a binary 1 when the switch is in the up position or a binary 0 when the switch is in the down position. Positioning of the 16 INFORMATION INPUT switches as directed by the tracking computer function troubleshooting procedures (TM 11-5840-271-30/9) causes a 16 bit word to be generated. Since all tracking computer function troubleshooting input data is given in octal code, all given input data must be converted to binary code to properly set the INFORMATION INPUT switches. Information in binary code is set on the INFORMATION INPUT switches exactly as the word is written. Output signals from each of the INFORMATION INPUT switches are gated to different P times between P0 and P15 and are entered serially into an enter information flip-flop. The enter information flip-flop is set true each P time that coincides with an INFORMATION INPUT switch in the true position; therefore, output signals from the flip-flop represent the complement of each digit of the selected 16 digit binary word. The enter information output signal is applied to the test band write flip-flop and represents the complement of the information word which must be entered in a preselected test band word slot during slot coincidence.

c. Test Band Information Loading. Test band information loading is provided by the ENTER INFO pushbutton S1 on the computer test control panel. The ENTER INFO pushbutton is pressed each time a new information word is loaded on the test band. Two output signals are provided by the ENTER INFO pushbutton; one output signal is true when the switch is operated and the other output signal is true when the switch is not operated. Both output signals are applied to the input of the test band write flip-flop. Depressing the ENTER INFO pushbutton causes the flip-flop to be set true each P time that the enter information flip-flop is set false during test band slot coincidence. Output signals from the test band write flip-flop represent the selected input information word and

are timed so that each digit of the information word enters the proper P digit position of the selected test band word slot. The output signals are routed to the test band. The manual entry band (test band) read flip-flop in the storage function (TM 11-5840-271-30/3) returns an output signal to the input of the test band write flip-flop to complete a path for recirculation. All information words entered on the test band remain unchanged until the ENTER INFO pushbutton is pressed to enter new information or until power is removed from the storage function. To check information entered into any test band slot, the SLOT SEL LSD and MSD switches S18 and S19 are set to the test band slot to be observed and the INFO SELECTOR switch on the computer test control panel is set to the TEST position. The display lamps directly above the INFORMATION INPUT switches then glow to indicate the binary word entered into the selected test band word slot.

10. Computer Test Display Selection
(fig. 3)

Computer test display selection is the operation required to initiate a particular computer test information display. This operation must be performed in accordance to tracking computer function troubleshooting procedures. Test information displays are initiated by first selecting the display condition, which also includes selection of a major cycle at which the display occurs. The test information to be displayed is then selected, and finally the tracking computer test computations are started. When this operation is completed, data control and data entry signals are developed and routed to the computer test function display register. Data control signals are developed as a result of display condition selection and are used to time the display register so that only the selected information word is displayed. Data entry signals route the selected test information to the display register. Initial tracking computer test computations are started after all test input information has been entered on the test band and the desired test information display has been selected. When test computations are started, the tracking computer automatically reads the test input information from the test band, transfers the information to the test sector, and performs a series of computations on the test information. The test sector is one word slot in each of the 44 computation bands used by the tracking computer, and is used to store computer test information.

a. Display Condition Selection. Display condition selection provides control of the display register so that test information being entered can only change the display register configuration at predetermined intervals. The display register is controlled by the output signal from a data control flip-flop which is set true when the selected display conditions occur. Three display conditions which set the data control flip-flop true are selected by operation of the INFO SELECTOR switch S20 and ONCE ONLY-EVERY DREV switch S24 located on the computer test control panel. When the INFO SELECTOR switch is in the TEST position, the data control flip-flop is set true by the slot coincidence signal so that only the information word occurring in the selected test band slot is displayed. If the INFO SELECTOR switch is in the PATCH position, the data control flip-flop is set true during the test sector OT word so that only test result information is displayed. Test result information is displayed during every DREV or during the selected major cycle as determined by the ONCE ONLY-EVERY DREV switch position. In the EVERY DREV position, a continuous display is provided because the data control flip-flop is set true during the test sector OT word of every DREV. During ONCE ONLY operation the selected cycle occurs before the data control flip-flop is set true.

b. Major Cycle Selection. Major cycle selection provides a fixed display of a test result information word which occurs at the selected major cycle. To obtain this display, the ONCE ONLY-EVERY DREV switch is set to the ONCE ONLY position and the major cycle at which the test result information occurs is selected by operating the major cycle selector switches on the computer test control panel. MAJOR CYCLE SEL TENS switch S33 selects major cycle tens digits from 0 through 6 and MAJOR CYCLE SEL UNITS switch S32 selects major cycles in units from 0 through 9. Combined operation of both switches allows any major cycle from 0 through 68 to be selected. P digit signals are applied to the contacts of the major cycle selector switches so that when any major cycle is selected, corresponding P digits which represent the selected major cycle are routed through the switches to a major cycle number compare flip-flop. The selected major cycle number is then compared to major cycle units and major cycle tens signals received from

the storage function and when major cycle coincidence occurs, the major cycle number compare output signal is true at P0 time of the test sector. The major cycle number compare output signal is routed to the data control flip-flop and to a major cycle subcycle Selector flip-flop. The data control flip-flop is set true to allow a test result information word to enter the display register and the major cycle subcycle selector flip-flop then immediately goes false to prevent the data control flip-flop from becoming true again until the selected major cycle reoccurs.

c. Test Information Selection. Test information to be displayed by the display register is selected by the INFO SELECTOR switch S20 and the patch board test probe S25 on the computer test function control panel. When the INFO SELECTOR switch is in the TEST position, the information entered on the test band is read from the test band into a data entry flip-flop. The output signals from the data entry flip-flop represent the test band information and are routed to the display register. Placing the INFO SELECTOR switch in the PATCH position allows computer test result information to be selected from the control panel patch board. The test point into which the patch board test probe S25 is inserted is determined by the tracking computer function troubleshooting procedure. After selecting the test point and inserting the test probe, the START COMPUTATION pushbutton S26 is pressed and during the computation cycle, information from the selected test point is routed to the data entry flip-flop. The data entry flip-flop output signals reflect the selected information and the information is routed to the display register. Only the information entering the display register while the data control flip-flop is true affects the display register configuration.

d. Computer Test Computation. Each time a new test results display is selected a series of tracking computer computations are required. These computations are initiated by pressing the START COMPUTATION pushbutton S26 on the computer test control panel. Start computation F/F31 is set true when the START COMPUTATION switch is operated and remains true until P14 time of the test sector when the test band slot counter is in octal state 37. At this time, the output of F/F31 is used to start the tracking computer computation cycle. During the next 31 DREVs test information words which were previously entered on the test band are transferred one word each DREV to the test sector by the tracking computer. The last word read from the test band is a major cycle constant which starts the tracking computer computation. Tracking computer computation continues until all calculations are performed for 68 major cycles. Test result information is read into the display register during any one of the 68 major cycles.

11. Computer Test Display Register
(fig. 4)

The computer test display register provides an on time (OT) display of any binary word which contains a maximum of 16 digits. Binary words displayed by the display register can be either computer test result information or test data input information. Computer test result information is routed through data entry F/F12 and a gate amplifier to the display register from the patch board test probe S25 on the computer test control panel. Test data input information is routed through data entry F/F12 and gate amplifiers to the display register from the storage function test band. Data entry signals (GQ12 and $G\bar{Q}12$) represent the input information and are routed to the display register input. Data control signal (GQ13) is also routed to the display register input. The data control signal inhibits the display register between selected information words so that only the selected information is displayed. The display register contains 16 display flip-flops which register the input information at preselected intervals, and each output signal from the 16 display flip-flops controls one lamp of a 16 lamp binary display.

a. Display Control. Display control is provided by the 16 display register flip-flops. Each of the 16 display flip-flops receives the data entry and the data control input signals. Data control signal (GQ13) is true at the inputs to all display flip-flops during the selected word times. Data entry signal GQ12 is applied to all J inputs of the display flip-flops and data entry signal $G\bar{Q}12$ is applied to all K inputs of the display flip-flops. These signals carry the information word but they do not cause any display flip-flop to change state until the proper P time occurs. One P time signal from P0 through P15 is received from the timing function (TM 11-5840-271-30/3) and applied to both the J and K inputs of each display flip-flop. When data control signal GQ13 is true and the P time for any display flip-flop occurs, the display flip-flop changes state

according to whether the data entry signal GQ12 or G$\overline{Q}$12 signal is true. The $\overline{Q}$ output from each display flip-flop is routed to an associated display lamp, since the $\overline{Q}$ signal provides a −6 volt state causing the lamp to glow when the flip-flop is set true.

b. Binary Display. The computer test binary display is provided by 16 indicator lamps which are individually controlled by the 16 display flip-flops. Each lamp represents one OT digit from P0 through P15 of a 16 bit word. When any lamp glows, a binary 1 is indicated in that digit position and when the lamp does not glow a binary 0 is indicated.

12. Computer Operating Mode Selection

(fig. 1)

Computer operating mode information is provided by the MAN MODE and AUTO MODE switches S27 and S28 on the computer test control panel. The MAN MODE switch is placed in the INOPERATIVE position to inform the DT consoles that information received from the manual track circuit is incorrect or the tracking computer is malfunctioning. With the MAN MODE switch S27 placed in the OPERATIVE position, the tracking computer functions in either the manual or automatic mode as selected by the AUTO MODE switch S28. The tracking computer operates in the automatic mode when the AUTO MODE switch is placed in the OPERATIVE position and is prevented from operating in automatic mode when the switch is placed in the INOPERATIVE position. Indicator lamps directly above each switch indicate the selected switch positions. Output signals from the switches are routed to the DT consoles data entry function, TM 11-5840-271-30/13 and to the tracking computer function, TM 11-5840-271-30/8.

13. Memory Clear

(fig. 1)

MEMORY CLEAR pushbutton S30 is located under a spring loaded door on the front panel of the computer test set and display control 501051. Depressing the MEMORY CLEAR pushbutton causes all recorded data to be removed from local memory action bands 1 through 6 and major cycle tens and minor cycle band. When the pushbutton is depressed an output signal is routed to the data exchange function TM 11-5840-271-30/2, DT consoles data entry function TM 11-5840-271-30/15, RHI consoles data entry function TM 11-5840-271-30/16, and to the tracking computer function TM 11-5840-271-30/8.

14. ARDME Data Reject

(fig. 4)

A REJECT ARDME DATA indicator lamp DS17 is located on the computer test control panel. The REJECT ARDME DATA indicator lamp glows only when an ARDME malfunction occurs. To light the REJECT ARDME DATA indicator lamp, an ARDME malfunction signal is received from the tracking computer function and routed to a pulse stretcher in the computer test function. The pulse stretcher then deenergizes a relay and holds the relay deenergized for two seconds. While the relay is deenergized, 28 volts applied to the REJECT ARDME DATA indicator lamp is routed through the relay contact to ground, causing the lamp to glow. After two seconds have elapsed, the relay returns to the normally energized position and the REJECT ARDME DATA indicator lamp does not glow. This sequence will continue until the ARDME malfunction signal is not received or until the tracking computer is placed in the manual operating mode.

Section II. COMPUTER TEST FUNCTION, DETAILED FUNCTIONAL THEORY

15. General

This section contains detailed functional descriptions and operation logic for the computer test function. The section is divided into paragraphs describing specific circuits and the circuit operation. All input signals received from and supplied to other functions are listed in paragraph 16. Computer test function flip-flops and logic are listed in paragraph 17.

16. Input and Output Signals

(fig. 22)

Paragraphs 16*a* and 16*b* list the signals supplied to the computer test function by other functions in the RDPC subsystem. Output signals supplied by the computer test function to other functions in the RDPC subsystem are listed in paragraph 16*c*.

a. Input Signals. The following chart lists the signals supplied to the computer test function except those used for test result displays. Test result display input signals are listed in paragraph *b*. The signals listed in this paragraph are listed numerically by the signal designation. The signal source and use by the computer test function is also listed.

Designation	Source	Use
$\bar{W}01$	Manual entry band (test band) read flip-flop from storage function TM 11-5840-271-30/5.	Recirculation logic for test band write flip-flop F/F33 and for test band information display.
W03	Test sector OT, from DT consoles data entry function TM 11-5840-271-30/5.	Routed to major cycle number compare flip-flop F/F30, major cycle subcycle selector flip-flop F/F32 and data control flip-flop F/F13 to provide timing for test results data display. W03 is true P0 through P15 of the test sector word.
W04	ARMDE malfunction, from tracking computer function TM 11-5840-271-30/8.	Provides signal which causes REJECT ARMDE DATA indicator lamp to glow. W04 is true for one word time during MC11 if the reject data digit (I_r) is true.
$\bar{W}05$	Major cycle units OWE, from the storage function.	Logic term for major cycle number compare flip-flop F/F30.
$\bar{W}06$	Major cycle tens and minor cycle OWE, from the storage function.	Logic term for major cycle number compare flip-flop F/F30.
W07	Test sector OWE, from DT consoles data entry function.	Logic term for major cycle number compare flip-flop F/F30. W07 is true P0 to P15 one word prior to the test sector word.

b. Patch Board Input Signals. The following chart lists the input signals supplied to the computer test function patch board. These signals are not used by the computer test function except to obtain a test result display. The signals are listed numerically according to the test points where the signal is applied. Designations of the signals refer to the computer test function designation and the signal name applies to the use of the signal by the tracking computer.

Test point	Designation	Name	Test point	Designation	Name
1	$\bar{W}101$	AU1 information $\bar{W}01$	18	$\bar{W}118$	First minor cycle
2	$\bar{W}102$	AU2 information $\bar{W}01$	19	$\bar{W}119$	Last minor cycle
3	$\bar{W}103$	AU3 information $\bar{W}01$	20	$\bar{W}120$	Constants generator 1
4	$\bar{W}104$	AU1 information $\bar{W}02$	21	$\bar{W}121$	Constants generator 2
5	$\bar{W}105$	AU2 information $\bar{W}02$	22	$\bar{W}122$	Constants generator 3
6	$\bar{W}106$	AU3 information $\bar{W}02$	23	$\bar{W}123$	Delay X_{DB}
7	$\bar{W}107$	AU1 information $\bar{W}03$	24	$\bar{W}124$	Delay Y_{DB}
8	$\bar{W}108$	AU2 information $\bar{W}03$	25	$\bar{W}125$	X display
9	$\bar{W}109$	AU3 information $\bar{W}03$	26	$\bar{W}126$	Y display
10	$\bar{W}110$	AU1 control A	27	$\bar{W}127$	Delay $\dot{X}$
11	$\bar{W}111$	AU2 control A	28	$\bar{W}128$	Delay $\dot{Y}$
12	$\bar{W}112$	AU3 control A	29	$\bar{W}129$	Delay Z_p
13	$\bar{W}113$	AU1 control C	30	$\bar{W}130$	$\epsilon\theta$
14	$\bar{W}114$	AU2 control C	31	$\bar{W}131$	Sign of $\epsilon\theta$
15	$\bar{W}115$	AU3 control C	32	$\bar{W}132$	$\Delta\theta$
16	$\bar{W}116$	AU1-3 control B	33	$\bar{W}133$	$\theta'p-(\theta i+K)$
17	$\bar{W}117$	AU1-3 control D	34	$\bar{W}134$	θi

Test point	Designation	Name
35	W135	Temporary I and A display 1
36	W136	Temporary I and A display 2
37	W137	Temporary I and A display 3
38	W138	Temporary I and A display 4
39	W139	Tracking computer mode
40	W140	Reject data
41	W141	Poor track
42	W142	Manual correction
43	W143	Minor cycle count LSD
44	W144	Minor cycle count 2d LSD
45	W145	Minor cycle count 3d LSD
46	W146	Minor cycle count MSD
47	W147	Major cycle count unit 0
48	W148	Major cycle count unit 1
49	W149	Major cycle count unit 2
50	W150	Major cycle count unit 3
51	W151	Major cycle count unit 4
52	W152	Major cycle count unit 5
53	W153	Major cycle count unit 6
54	W154	Major cycle count unit 7
55	W155	Major cycle count unit 8
56	W156	Major cycle count unit 9
57	W157	Major cycle count tens 0
58	W158	Major cycle count tens 1
59	W159	Major cycle count tens 2
60	W160	Major cycle count tens 3
61	W161	Major cycle count tens 4
62	W162	Major cycle count tens 5
63	W163	Major cycle count tens 6
64	W164	Result band 1
65	W165	Result band 2
66	W166	Result band 3
67	W167	R_p
68	W168	X_p
69	W169	Y_p
70	W170	R_{1p}
71	W171	Xsm
72	W172	Ysm
73	W173	ρ_p
74	W174	ϕ'_p
75	W175	h′
76	W176	θ'_p
77	W177	θ''_p
78	W178	Temporary storage band 1
79	W179	Temporary storage band 2
80	W180	Temporary storage band 3
81	W181	Temporary storage band 4
82	W182	Temporary storage band 5
83	W183	T time
84	W184	T_1 time
85	W185	T_2 time
86	W186	$\Sigma\Delta\phi$
87	W187	$\Sigma\Delta\bar{R}$
88	W188	$\Sigma\Delta\theta$
89	W189	ΣH
90	W190	Action band 5 OT
91	W191	Action band 6 OT
92 through 102		Spares

c. Output Signals. The following chart lists the output signals supplied by the computer test function to other functions in the RDPC subsystem. Signal names and functions which receive each signal are also listed.

Designation	Name	Destination
Q05, $\bar{Q}05$	Test band slot counter LSD.	Tracking computer function (TM 11-5840-271-30/8).
Q06, $\bar{Q}06$	Test band slot counter 2d LSD.	Tracking computer function.
Q07, $\bar{Q}07$	Test band slot counter 3d LSD.	Tracking computer function.
Q08, $\bar{Q}08$	Test band slot counter 4th LSD.	Tracking computer function.

Designation	Name	Destination
Q09, $\bar{Q}$09	Test band slot counter MSD.	Tracking computer function.
Q31	Start computation	Tracking computer function.
Q33, $\bar{Q}$33	Test band write	Storage function (TM 11-5840-271-30/3).
S27-01	Manual mode operative	DT consoles received information function (TM 11-5840-271-30/13).
S28-01	Automatic mode operative.	DT consoles received information function.
S28-02	Automatic mode inoperative.	DT consoles received information function.
S30-03	Clear memory	Data exchange function (TM 11-5840-271-30/2), DT consoles data entry function (TM 11-5840-271-30/15), RHI Data entry function (TM 11-5840-271-30/16), Tracking computer function (TM 11-5840-271-30/8).

17. Flip-Flop Logic

The following chart lists the flip-flops contained in the computer test function. Fip-flops are listed in numerical order according to the flip-flop designation. Logic is given for both the J and K input terminal of each flip-flop and the flip-flop names are also listed.

Designation	Name	Logic
F/F05	Test band slot counter, LSD	J05 = $\bar{Q}$05 P14 K05 = Q05 ($\bar{Q}$06 + $\bar{Q}$07 + $\bar{Q}$08 + $\bar{Q}$09) P14
F/F06	Test band slot counter, 2d LSD	J06 = $\bar{Q}$06 Q05 P14 K06 = Q06 Q05 P14
F/F07	Test band slot counter, 3d LSD	J07 = $\bar{Q}$07 $\bar{Q}$06 Q05 P14 K07 = Q07 Q06 Q05 P14
F/F08	Test band slot counter, 4th LSD	J08 = $\bar{Q}$08 Q07 Q06 Q05 P14 K08 = Q08 Q07 Q06 Q05 P14
F/F09	Test band slot counter, MSD	J09 = $\bar{Q}$09 Q08 Q07 Q06 Q05 P14 K09 = Q09 Q08 Q07 Q06 Q05 P14
F/F10	Slot coincidence	J10 = S18-01 S18-02 S18-03 S19-01 S19-02 K10 = Q10 P15
F/F11	Enter information	J11 = $\bar{K}$11 K11 = (S02-01 P15) + (S03-01 P0) + (S04-01 P01) + (S05-01 P02) + (S06-01 P03) + (S07-01 P04) + (S08-01 P05) + (S09-01 P06) + (S10-01 P07) + (S11-01 P08) + (S12-01 P09) + (S13-01 P10) + (S14-01 P11) + (S15-01 P12) + (S16-01 P13) + (S17-02 P14)
F/F12	Data entry	J12 = $\bar{K}$12 K12 = (S20-01 S25-01) + (S20-02 $\bar{W}$01)

Designation	Name	Logic
F/F13	Data control	J13 = (S20–01 Q30 $\bar{Q}$32 W03 P0) + (S20–01 S24–01 W03 P0) + (S20–02 Q10) K13 = P0 Q13
F/F14	Display register LSD	J14 = GQ12 P01 G1Q13 K14 = G$\bar{Q}$12 P01 G1Q13
F/F15	Display register 2d LSD	J15 = GQ12 P02 G1Q13 K15 = G$\bar{Q}$12 P02 G1Q13
F/F16	Display register 3d LSD	J16 = GQ12 P03 G1Q13 K16 = G$\bar{Q}$12 P03 G1Q13
F/F17	Display register 4th LSD	J17 = GQ12 P04 G1Q13 K17 = G$\bar{Q}$12 P04 G1Q13
F/F18	Display register 5th LSD	J18 = GQ12 P05 G1Q13 K18 = G$\bar{Q}$12 P05 G1Q13
F/F19	Display register 6th LSD	J19 = GQ12 P06 G1Q13 K19 = G$\bar{Q}$12 P06 G1Q13
F/F20	Display register 7th LSD	J20 = GQ12 P07 G1Q13 K20 = G$\bar{Q}$12 P07 G2Q13
F/F21	Display register 8th LSD	J21 = GQ12 P08 G1Q13 K21 = G$\bar{Q}$12 P08 G1Q13
F/F22	Display register 9th LSD	J22 = GQ12 P09 G2Q13 K22 = G$\bar{Q}$12 P09 G2Q13
F/F23	Display register 10th LSD	J23 = GQ12 P10 G2Q13 K23 = G$\bar{Q}$12 P10 G2Q13
F/F24	Display register 11th LSD	J24 = GQ12 P11 G2Q13 K24 = G$\bar{Q}$12 P11 G2Q13
F/F25	Display register 12th LSD	J25 = GQ12 P12 G2Q13 K25 = G$\bar{Q}$12 P12 G2Q13
F/F26	Display register 13th LSD	J26 = GQ12 P13 G2Q13 K26 = G$\bar{Q}$12 P13 G2Q13
F/F27	Display register 14th LSD	J27 = GQ12 P14 G2Q13 K27 = G$\bar{Q}$12 P14 G2Q13
F/F28	Display register 15th LSD	J28 = GQ12 P15 G2Q13 K28 = G$\bar{Q}$12 P15 G2Q13
F/F29	Display register MSD	J29 = GQ12 P0 G2Q13 K29 = G$\bar{Q}$12 P0 G2Q13
F/F30	Major cycle number compare	J30 = W03 K30 = (S32–01 $\bar{W}$05 W07) + (S33–01 W06 W07)
F/F31	Start computation	J31 = S26–01 (differentiated) K31 = Q31 Q05 Q06 Q07 Q08 Q09 P14 W03
F/F32	Major cycle subcycle selector	J32 = (Q30 W03 P0) + (S24–01 W03 P0) K32 = Q31
F/F33	Test band write	J33 = $\bar{K}$33 K33 = (Q10 $\bar{Q}$11 S01–02) + ($\bar{Q}$10 $\bar{W}$01) + (S01–01 $\bar{W}$01)

18. Test Band Slot Selection
(fig. 5)

The test band is divided into 31-word slots which are used to store information words preparatory to performing a tracking computer test. For each tracking computer test to be performed, 22 information words are entered on the test band by the computer test function. Each information word entered on the test band must be entered in a particular test band slot, because each test band slot has a unique relationship to the tracking computer computations. The purpose of the test band slot selection circuit is to provide accurate test band slot coincidence signals to the information input circuit so that each information word may be entered in a predetermined test band slot. The test band slot selection is provided by a test band slot counter and a slot coincidence circuit.

a. Test Band Slot Counter. The test band slot counter consists of F/F05 through F/F09. Logic equation for these flip-flops are given in paragraph 17. F/F05 provides the LSD slot count and F/F09 provides the MSD slot count. A P14 time signal supplies the timing for the test band slot counter so that at each P15 time the counter output changes configuration. The test band slot counter counts continuously from binary 1 through binary 31, resets to binary 1, and then repeats the counting sequence. K input logic for F/F05 prevents the test band slot counter from resetting to zero and, except for this logic, the counter is similar to a mod 32 counter. The Q and the $\overline{Q}$ output signals from the five slot counter flip-flops are used in the computer test function for test band slot selection and start computation timing, and are amplified and used by the tracking computer and ARDME functions for identifying test band slots. A chart listing the test band slot counter output signals routed to the tracking computer and ARDME functions is shown on figure 22, sheet 3 of 3.

b. Test Band Slot Coincidence Circuit. The test band slot coincidence circuit contains the SLOT SEL LSD and SLOT SEL MSD switches S18 and S19 and slot coincidence F/F10. Slot count output signals from the test band slot counter are routed to the contacts of the slot selector switches. SLOT SEL LSD switch S18, a three wafer rotary switch, has the Q and $\overline{Q}$ output signals from one slot counter flip-flop connected to contacts of each wafer. The output signal from each wafer reflects either the Q or $\overline{Q}$ signal depending upon the selected switch position. Output signal S18–01 reflects the LSD output from F/F05, S18–02 reflects the second LSD output from F/F06, and S18–03 reflects the third LSD output from F/F07. SLOT SEL MSD switch S19, a double pole single wafer switch, provides output signals S19–01 and S19–02. Output signal S19–02 reflects the fourth LSD output from F/F08 and S19–01 reflects the MSD output from F/F09. The five output signals from the slot selector switches are routed to the J input of the slot coincidence F/F10. Flip-flop F/F10 is set true when all five slot selector switch outputs are true. This condition occurs when the slot counter configuration is the same as the test band slot selected by the slot selector switches. The following chart shows the selected test band slot in octal code, slot counter configuration at coincidence in binary code, and the decimal equivalent.

Selected test band slot in octal code		Slot counter configuration at slot coincidence (Binary 1 indicates Q output is true and binary 0 indicates $\overline{Q}$ output is true)					Decimal equivalent
SLOT SEL MSD switch position	SLOT SEL LSD switch position	F/F09	F/F08	F/F07	F/F06	F/F05	
0	0	No coincidence at this switch position					0
0	1	0	0	0	0	1	1
0	2	0	0	0	1	0	2
0	3	0	0	0	1	1	3
0	4	0	0	1	0	0	4
0	5	0	0	1	0	1	5

Selected test band slot in octal code		Slot counter configuration at slot coincidence (Binary 1 indicates Q output is true and binary 0 indicates $\overline{Q}$ output is true)					Decimal equivalent
SLOT SEL MSD switch position	SLOT SEL LSD switch position	F/F09	F/F08	F/F07	F/F06	F/F05	
0	6	0	0	1	1	0	6
0	7	0	0	1	1	1	7
1	0	0	1	0	0	0	8
1	1	0	1	0	0	1	9
1	2	0	1	0	1	0	10
1	3	0	1	0	1	1	11
1	4	0	1	1	0	0	12
1	5	0	1	1	0	1	13
1	6	0	1	1	1	0	14
1	7	0	1	1	1	1	15
2	0	1	0	0	0	0	16
2	1	1	0	0	0	1	17
2	2	1	0	0	1	0	18
2	3	1	0	0	1	1	19
2	4	1	0	1	0	0	20
2	5	1	0	1	0	1	21
2	6	1	0	1	1	0	22
2	7	1	0	1	1	1	23
3	0	1	1	0	0	0	24
3	1	1	1	0	0	1	25
3	2	1	1	0	1	0	26
3	3	1	1	0	1	1	27
3	4	1	1	1	0	0	28
3	5	1	1	1	0	1	29
3	6	1	1	1	1	0	30
3	7	1	1	1	1	1	31

When slot coincidence F/F10 is set true it remains true for one word time (P0 to P15) and is then set false until slot coincidence reoccurs. Slot coincidence signals (Q10 and $\overline{Q}10$) are routed to test band write F/F33. Q10 is used in the logic equation for entering new information on the test band and $\overline{Q}10$ is used in the recirculation logic to recirculate the information entered previously.

19. Test Information Entry

(fig. 6)

Twenty-two information words are required to initiate a tracking computer test. Each of these words is generated and entered one at a time into a selected word slot on the test band. The information word to be generated and the particular word slot in which it must be entered is determined by the tracking computer troubleshooting procedure. Test information entry is accomplished by an information input circuit and test band write circuit.

a. Information Input Circuit. The information input circuit consists of the 16 INFORMATION INPUT P0–P15 switches S02–S17 and enter information flip-flop F/F11 INFORMATION INPUT switches S02 through S17 are all single-pole single-throw switches which are identical in operation. In the up position the output signal from each switch is false which causes a binary 1 to be generated, and

in the down position the output signal is true which causes a binary 0 to be generated. Each switch represents one digit of a 16 bit word. The tracking computer troubleshooting procedure is given in octal code, so it is necessary to convert the given data to the binary system to properly set the INFORMATION INPUT switches. When all the switches are set as directed, a 16 bit word is generated at the switch outputs. INFORMATION INPUT switch output signals S02–01 through S17–01 are each anded with a different P time so that every output signal is serially presented to the enter information flip-flop K input. Logic for enter information F/F11 is given in paragraph 17. The enter information flip-flop is set true for one bit time for each P time anded with a true switch signal. All switch outputs are presented to the enter information flip-flop one P time early to compensate for the one P time delay between the flip-flop input and output. $\bar{Q}11$ output represents the complement of the information word set by the INFORMATION INPUT switches with each digit on time (OT). $\bar{Q}11$ is routed to test band write flip-flop F/F33 where it is used in the logic term for entering new information on the test band.

b. Test Band Write Circuit. The test band write circuit consists of ENTER INFO switch S1 and test band write flip-flop F/F33. The ENTER INFO switch is a double-pole single-throw push button switch, provides output signals S01–01 and S01–02. Output signal S01–01 is true when the switch is not operated and false when the switch is operated. Output signal S01–02 is the complement of the S01–01 output. Both ENTER INFO switch output signals are routed to test band write F/F33. Output signal S01–02 is used in the logic term for entering new information on the test band and S01–01 is used in the recirculation logic. Logic for test band write F/F33 is given in paragraph 17. ENTER INFO switch S1 is operated to enter a new information word into a selected test band slot. When the switch is operated F/F33 is set true each P time F/F11 is set false during slot coincidence. Slot coincidence signal (Q10) is true at F/F33 input from P0 to P15 OT of the selected word slot. Due to the one P digit delay in F/F33, the information word routed to the storage function is written on the test band from P01 OT to P0 OWL. The manual entry band (test band) read signal $\bar{W}01$ from the storage function is routed to F/F33 input to provide a recirculation path. $\bar{W}01$ is anded with both the slot coincidence $\bar{Q}10$ signal and the ENTER INFO switch S01–01 signal. The $\bar{Q}10$ signal provides recirculation of entered information while the ENTER INFO switch is operated, and the S01–01 signal provides recirculation while the ENTER INFO switch is not operated. Information entered on the test band will remain unchanged until new information is entered or until power is removed from the storage function. Test band write output signal Q33 represents the 16 bit word set on the INFORMATION INPUT switches and $\bar{Q}33$ represents the complement of Q33.

20. Data Display Control

Data display control is provided by a major cycle selection circuit and a data control circuit. A data control signal developed by these circuits is used to inhibit the display register at all times except when the selected display conditions occur. Display conditions are selected in accordance with tracking computer function troubleshooting procedures TM 11–5840–271–30/9 to obtain a specific display.

a. Major Cycle Selection Circuit. The major cycle selection circuit contains MAJOR CYCLE SEL UNITS switch S32, MAJOR CYCLE SEL TENS switch S33, and major cycle number compare F/F30, (fig. 9). The major cycle selection switches are rotary type switches used to select a tracking computer major cycle at which a particular test results display is to be observed. P time signals are applied to the contacts of the major cycle selection switches. By setting the switches to a particular major cycle, combinations of the applied P time signals are selected, and when the selected P time occurs, output signals from the major cycle selection switch represent the selected major cycle. MAJOR CYCLE SEL UNITS switch S32 selects P times from P0 through P09 and the switch output signal S32–01 represents the unit portion of the selected major cycle from 0 through 9. MAJOR CYCLE SEL TENS switch S33 selects P times from P0 through P06 and the switch output signal S33–01 represents the tens portion of the selected major cycles from 0 through 6. Combined use of both switches provides selection of tracking computer major cycles from 0 through 68. Major cycle units output signal S32–01 and major cycle tens output signal S33–01 are both routed to major cycle number compare F/F30. Logic for F/F30 is given in paragraph 17. Four external signals are also used in the

logic for F/F30. Major cycle units signal $\overline{W}05$ and major cycle tens and minor cycle signal $\overline{W}06$ are supplied by the storage function, and test sector OT signal W03 and test sector OWE signal W07 are supplied by the DT consoles data entry function. W03 sets F/F30 true at P0 time of the test sector but the flip-flop output signal Q30 does not go true until P01 time of the test sector. Every DREV until the selected major cycle occurs, F/F30 is set false one word prior to the test sector at the P time selected by the major cycle selection switches. This prevents F/F30 from being true during P0 time of the test sector until the selected major cycle occurs. When the selected major cycle occurs, either $\overline{W}05$ or $\overline{W}06$ goes false and major cycle number compare output signal Q30 remains true until the test sector OWE signal W07 reoccurs. F/F30, output signal Q30 is true during PO time of the test sector to provide data display control at the selected major cycle. The Q30 output is routed to major cycle subcycle selector F/F32, and to data control F/F13.

b. Data Control Circuit. The data control circuit contains ONCE ONLY-EVERY DREV switch S24, major cycle subcycle selector F/F32, and data control F/F13. Output signals from INFO SELECTOR switch S20 are also used in the data control circuit logic terms. When S20 is set in the TEST position, slot coincidence signal Q10 provides the logic for data control, and when S20 is in the PATCH position, data control logic is provided by S24. ONCE ONLY-EVERY DREV switch S24 is a single-pole single-throw switch with output signal S24–01 true in the EVERY DREV position and false in the ONCE ONLY position. S24–01 is used in the logic of data control F/F13 and major cycle subcycle selector F/F32 for selecting display conditions of test result information. Complete logic for F/F13 and F/F32 is given in paragraph 17. When ONCE ONLY-EVERY DREV switch is placed in the ONCE ONLY position, major cycle subcycle selector F/F32 detects the first occurring minor cycle of the slected major cycle. To do this, F/F32 is set false when the tracking computer starts the computation cycle and remains false until P0 time of the test sector when the selected major cycle occurs. At this time, F/F32 is set true and the $\overline{Q}32$ output signal is set false one P time later. F/F13 is also set true at P0 time of the test sector and remains true for one word time but, because $\overline{Q}32$ is now a false term in the logic of F/F13, the data control flip-flop cannot become true again until the next selected major cycle occurs. Since F/F13 must be true for the display register to change configuration, the display register only contains the test result information entered during the selected major cycle. When S24 is placed in the EVERY DREV position, F/F13 is set true each occurring P0 time of the test sector. F/F32 is also set true at the first occurring test sector P0 time but $\overline{Q}32$ is not used. This condition allows the display register to change configuration according to the test result information being entered during every DREV. Test band input information can only enter the display register when INFO SELECTOR switch S20 is placed in the TEST position. Slot coincidence signal Q10 then provides the logic that sets F/F13 true and allows the input information word to be entered in the display register. F/F13 never remains true for longer than one word time.

21. Display Data Entry

(fig. 9)

Display data entry is provided by a data entry circuit and a start computation circuit. The start computation circuit causes transfer of test information from manual entry band test sector bands of drum memory. Output signals from the data entry circuit are representative of the input or test result information and are routed to the display register to provide a display of the selected information.

a. Data Entry Circuit. The data entry circuit contains INFO SELECTOR switch S20, the control panel patch board, and data entry F/F12. The INFO SELECTOR switch S20, a double-pole double-throw switch, supplies output signals S20–01 and S20–02. S20–01 is true when the switch is in the PATCH position and false when the switch is in the TEST position. S20–02 is true when the switch is in the TEST position and false when the switch is in the PATCH position. Both output signals are routed to data entry F/F12. Logic for F/F12 is given in paragraph 17. When INFO SELECTOR switch S20 is in the TEST position, all information entered on the the test band is read into F/F12 by manual entry band (test band) read signal $\overline{W}01$. Test result information is read into F/F12 when the INFO SELECTOR switch S20 is in the PATCH position. The patch board test probe is inserted into a preselected test point to obtain test result information, and the test probe

output signal S25–01 routes the selected information to F/F12. All tracking computer test information routed to the patch board is listed in paragraph 16. All information routed to F/F12 is represented by the flip-flop output signals Q12 and $\overline{Q}12$. Both Q12 and $\overline{Q}12$ output signals are amplified and then routed to the display register as GQ12 and G$\overline{Q}12$.

b. Start Computation Circuit. The start computation circuit contains START COMPUTATION pushbutton S26 and start computation flip-flop F/F31. Output signal S26–01 form S26 is true when the pushbutton is not depressed and false when the pushbutton is depressed. When S26 is depressed, the false output signal is routed to the J′ input terminal of start computation F/F31. The flip-flop is set true immediately and remains true until P14 time of the test sector when the test band slot counter is in octal state 37. Logic for start computation F/F31 is listed in paragraph 17. Output signal Q31 is routed to the tracking computer function, and the tracking computer begins the test computation cycle just as F/F31 is being set false. When the test computation cycle starts, a series of operations is performed by the tracking computer. Input information words are read serially from the test band into the ARDME and tracking computer functions. In these functions, each information word is gated into different write flip-flops which then rewrite each of the words in parallel form on the memory bands used by the tracking computer. If takes 31 DREVs to complete this operation because only one test band word is transferred during each DREV. The group of slots on the memory bands which are used to store computer test information is called the test sector. The last word to be read from the test band is a major cycle constant and is used to start the tracking computer computation program. Program steps may begin at major cycle 1 or major cycle 25 depending upon the information word entered in the test band slot 37. Once the program starts, the tracking computer continues the program through each of the 68 major cycles and returns to major cycle 0, which is the rest state. To read test result information at any major cycle, that major cycle and the information to be read is selected before starting the computation cycle. And each time a different test point or new major cycle is selected, the computation cycle is repeated by depressing the START COMPUTATION pushbutton.

22. Display Register

(fig. 10)

The computer test function provides an on time (OT) binary display by 16 display indicator lamps. Each lamp is individually controlled by one of 16 display register flip-flops. The logic for display registers F/F14 through F/F29, is listed in paragraph 17. All display register flip-flops receive gate amplified data control signal GQ13 at both the J and K inputs, gate amplified data entry signal GQ12 at the J input, and gate amplified data entry signal G$\overline{Q}12$ at the K input. Data control signal GQ13 is true for one word time, from P01 OT-P0 OWL during either the test sector or the selected test band word slot. In either case, an information word is read into the display register while GQ13 is true and the display register is inhibited at all other times. Data entry signals GQ 12 and G$\overline{Q}12$ route the input information to the display register. This information may be from selected patch board test point or from the manual entry band (test band), and all information occurring at these points is presented to the display register. However, the display register only accepts the information presented when data control signal GQ13 is true. Timing for the display register is provided by P time signals. Each flip-flop receives a different P time signal which is applied to the J and K inputs so that the flip-flop cannot change state unless the associated P time is present. Output signals from the flip-flops are all $\overline{Q}$ signals, each of which are routed to one display indicator lamp. The $\overline{Q}$ output signal is used because it provides the −6 volts necessary to cause the display lamp to glow when the flip-flop is set true. Each of the 16 display indicator lamps provide one digit of a 16 bit word. The word bits displayed by the display indicator lamps are on time with each word bit presented to data entry F/F12. This is accomplished through the mounting arrangement of the display lamps on the control panel.

23. Computer Operating Mode Selection Circuit

(fig. 22)

The computer operating mode selection circuit contains MAN MODE switch S27, AUTO MODE switch S28, MAN MODE indicator lamp DS18, and AUTO MODE indicator lamp DS19. MAN MODE switch S27 supplies manual mode operative signal S27–01, manual mode inoperative signal S27–02, and a signal which causes the MAN

MADE indicator lamp to glow. S27–01 is false and S27–02 is true when the switch is in the INOPERATIVE postion and DS18 does not glow. With the MAN MODE switch in the OPERATIVE position, S27–01 is true, S27–02 is false, and DS18 glows. All MAN MODE switch signals are routed to the contacts of AUTO MODE switch S28 to provide control over the S28 output signals. If S27 is placed in the INOPERATIVE position, signal S27–02 is routed to contacts of S28 and forces automatic mode inoperative signal S28–02 to be true in either AUTO MODE switch position. Signal S27–01 is also routed to S28 contacts and forces automatic mode operative signal S28–01 to be false in either AUTO MODE switch position. Placing S27 in the OPERATIVE position allows S28–01 to be false and S28–02 to be true when S28 is in the INOPERATIVE position and S28–01 to be true and S28–02 to be false when S28 is in the OPERATIVE position. DS19 glows only when both switches are in the OPERATIVE position. Manual mode operative signal S27–01 and automatic mode operative signal S28–01 are routed to the DT consoles data entry function (TM 11–5840–271–30/13) to provide computer operating mode information. Automatic mode operative signal S28–01 and automatic mode inoperative signal S28–02 are routed to the tracking computer function (TM 11–5840–271–30/8) and are used in logic terms to either allow or prevent the computer from operating in the automatic mode.

24. Clear Memory Circuit

(fig. 22)

The clear memory circuit contains CLEAR MEMORY pushbutton S30 which is located under a spring loaded door on the front panel of the 501051 unit. S30 has two output signals; S30–03 and S30–04. S30–03 is false when the pushbutton is not depressed and true when the pushbutton is depressed. S30–04 is true when the pushbutton is not depressed and false when the pushbutton is depressed. Depressing CLEAR MEMORY pushbutton S30 causes binary zeros to be written in all digit positions on actions bands 1, 2, 3, 5, and 6 and the major cycle tens and minor cycle band of the storage function. Signal S03-03 is routed to the data exchange function, DT consoles data entry function, RHI data entry function, and the tracking computer function. S03–04 is not used.

25. Reject ARDME Data Circuit

(fig. 22)

The reject ARDME data circuit contains the REJECT ARDME DATA indicator lamp on the control panel and an ARDME malfunction pulse stretcher circuit. When an ARDME malfunction is detected by the tracking computer, an ARDME malfunction signal is routed to the computer test function. ARDME malfunction signal W04 is true for one word time during major cycle 11 if the tracking computer reject data digit (Ir) is true. When an ARDME malfunction signal is received by the computer test set, it is routed to the ARDME malfunction pulse stretcher. The pulse stretcher contains an astable multivibrator, an npn switching transistor, and a relay. The relay is normally held in the energized position by the switching transistor. Receiving an ARDME malfunction signal starts the multivibrator which back biases the switching diode causing the relay to become deenergized. Deenergizing the relay allows 28 volts to be applied through the indicator lamp and the relay contacts to ground. The REJECT ARDME DATA indicator lamp then glows until the multivibrator returns to the rest state and the relay reenergizes. When ARDME is malfunctioning the REJECT ARDME DATA lamp blinks on and off with an on time of two seconds and an off time of one second.

CHAPTER 3
DIGITAL DATA DISPLAY FUNCTION, THEORY OF OPERATION

Section I. GENERAL THEORY

26. General

This section contains general information related to operation of the digital data display function. The section is divided into paragraphs which describe each of the operations. Paragraph 27 identifies the units which are contained in the function and their location within the RDPC subsystem. Paragraph 28 lists all the switches and indicators used during the operational procedures and the remaining paragraphs provide operational information.

27. Description

(fig. 11)

The digital data display function is built-in test equipment used primarily to locate malfunctions in the RDPC subsystem digital circuits. The function consists of portions of two units which are listed numerically in the following chart. The common name, physical location, and content of each unit is also listed.

Manufacturer's part No.	Common name	Group	Reference designation	Level	Content
501051	Computer test set and display control.	30, 48	44	B	Contains the digital data display control panel.
501056	Display test set and computer test control.	30, 48	49	A and B	Contains circuits of the digital data display function including the program step selector with major and minor cycle selection switches.

28. Switches and Indicators

The following chart provides a list of all switches and indicators used during operation of the digital data display function. All but three of the switches and indicators listed are mounted on the digital data display control panel located in level B of the computer test set and display control 501051. The MAJOR TENS, MAJOR UNITS, and MINOR switches are mounted on the TCC STEP SELECTOR which is located in level B of the display test set and computer test control 501056. Each switch or indicator is listed in alphabetical order according to the panel nomenclature with the numerical designation, output signal designations, and the use of each switch or indicator also listed.

Nomenclature	Switch designation	Output signal designations	Use
DISPLAY GATE TIMING SN—SPECIAL.	S02	S02–01, S02–02.	Selects either sector number timing or special gate timing.

Nomenclature	Switch designation	Output signal designations	Use
DISPLAY REGISTER	DS01 through DS16.	Indicator lamps.	Presents visual display of information word contained in the display register flip-flops.
MAJOR TENS—OFF	S2	S2A–01, S2B–01.	Used in program step selection to select the major cycle tens count.
MAJOR UNITS	S1	S1–01	Used in program step selection to select the major cycle units count.
MINOR	S3	S3A–01, S3B–01, S3C–01, S3D–01.	Used in program step selection to select the minor cycle of a selected major cycle count.
Patch board test probe	S12	S12–01	Used to select the input test data to be presented to the display register.
SN ELECT	S04 through S10.	S04–01 and S04–02 through S10–01 and S10–02.	Selects the memory band sector containing an information word to be displayed.
SPECIAL GATE	A1 through A8	S03–01 through S03–08.	Used to patch in timing signals which will provide a digital display.
START DISPLAY	S01	S01–01	Operated to start display action.
CONTINUOUS HOLD	S11	S11–01	Controls repetition of the selected display.

29. Test Data Selection

(fig. 12)

The digital data display function allows visual examination of digital data for test purposes. Digital data to be displayed is selected from either the patch board on the 501051 unit control panel or from any digital data circuit which is timed by the same clock pulse. Patch board test points provide test data selection from storage function memory bands and the patch board test probe is also used to connect other digital circuits to the data input circuits. The patch board test probe is always connected to the $\overline{Q}$ output or equivalent of any digital circuit being tested in order to maintain the relationship between the binary information being displayed and the display register indicator lamps. When the patch board test probe is connected to any source of digital information, the digital information is routed by test probe output signal S12–01 to the imput of the data input F/F07. F/F07 follows the digital changes information applied to the input and state as the digital information changess tate. Output signals from F/F07 are routed to the display register where, when the display control signal is true, control the configuration of the display register according to the digital information being received.

30. Input Data Timing

(fig. 13)

To provide a binary display of test information, timing for the input data is established so that only the particular information desired is displayed. The input data timing to be used depends upon the binary information to be displayed. When input data is selected from the patch board, the DISPLAY GATE TIMING switch S02 is placed in the SN position and the timing is selected by positioning sector number selection switches. If input data is selected from a digital circuit other than the patch board, S02 is placed in the SPECIAL position and timing signals are then patched into the special gate test jacks to provide timing for that particular input data. Additional timing is provided when input data is received from either the patch board or a digital circuit and the particular information to be displayed occurs during a major cycle. This timing

is selected by operation of the major and minor cycle selection switches on the TCC STEP SELECTOR.

a. Sector Number Selection. Sector number selection is used when the test input information is taken from the patch board. The patch board signals are routed to the patch board from the storage function memory bands. The storage function memory bands are divided into 100 sectors (word slots) each containing a 16 digit binary word. Each patch board test point receives all the information read from one memory band. Seven SN SELECT switches mounted on the digital data control panel, are used to select any memory band sector from 1 through 100. Each of the seven SN selection switches provides one digit of a seven digit binary number, so when any switch is in the up position a binary 1 is indicated in that digit position and a binary 0 is indicated in any digit position where the switch is down. The sector number LSD is provided by the switch on the right and the MSD by the switch on the left. For example; when selecting the binary number 0110101, which represents SN53 in decimal numbers, the LSD, third LSD, fifth LSD, and sixth LSD switches are placed in up position and the second LSD, fourth LSD, and MSD switches remain down. Output signals from the seven sector number selection switches are anded with P times from P09 through P15 and the signals are then routed to the input data timing F/F06. F/F06 is prevented from becoming true during P0 of any sector until the selected sector number coincides with sector number signals received from the timing function. When F/F06 is true during P0, input data which occurs during that sector is allowed to change the display register configuration.

b. Special Gate Input Selection. Special gate input selection is used when the test input information is taken from any digital circuit other than the memory bands. Display conditions or timing signals which determine when a particular information word occurs, are selected from test points in the RDPC subsystem and jumpered to the SPECIAL GATE input test jacks. Any number of signals from 1 to 8 may be connected to separate SPECIAL GATE test jacks; however, all signals connected to the test jacks must be set true for at least one P time one word prior to the desired display. When this occurs the input data timing flip-flop is set true and remains true during P0 and the input data occurring at that word time changes the display register configuration.

c. Program Step Selection. Program step selection is used when the input data occurs at a particular major cycle or a minor cycle of a selected major cycle. A major cycle can be selected when either sector number or special gate timing is used; however, major cycles cannot be selected when a one word early (OWE) input data signal is being received. This is because the major cycle signals are being received OWE and do not have time to act on the received information. Program steps are selected by operation of the MAJOR UNITS, MAJOR TENS, and MINOR switches S1, S2, and S3 located on the TCC STEP SELECTOR in the 501056 unit. The MAJOR UNITS switch S1 selects major cycles from 0 through 9 in units and the MAJOR TENS switch selects major cycles from 0 through 6 in tens so, by combined operations of both switches, major cycles from 0 through 68 are selected. An off position is also provided on the MAJOR TENS switch S2 so that when program step selection is not being used, the switch is placed in the fully counterclockwise position. Input data which occurs at a minor cycle of a selected major cycle is displayed when the MINOR switch S3 is set to a position from 1 through 12 that indicates the minor cycle at which the information occurs. When a major cycle is selected, an output signal from the program step selector is routed to the input data timing F/F06 and this signal, which is true until major cycle coincidence occurs, prevents F/F06 from being set true. Major cycle coincidence always occurs OWE and at this time the program step selector output signal is false. F/F06 is then controlled by the output signals from either the sector number selection switches or the special gate.

31. Display Control

(fig. 14)

Display control provides control of the display register so that only one particular word (16 digits) of the input data causes a change in the display register configuration and then only at the selected intervals. Display intervals are set by operation of the continuous hold switch S11. When this switch is placed in the hold position, the display register is inhibited after the first input data word enters, and provides a display of the first word until new data is entered. If S11 is placed in the continuous position, the display register changes configuration each time

the input data source changes during the preselected timing conditions. After the input data source is connected to the digital data display input, input data timing signals are selected, and all switches set to provide a desired display, the STAR DISPLAY pushbutton S01 is depressed. Digital data display action does not begin until S01 is depressed, and then, when F/F06 is true during P0, display control F/F08, is set true at P0. The display control output signal goes true at P01 on time and remains true until P0 one word late. This output signal is routed to display register flip-flops and prevents the display register from changing configuration except when the signal is true.

32. Display Register

(fig. 12)

The display register, which provides a digital display of the input data entered at preselected times, consists of 16 display indicator lamps DS01-DS16 and 16 display registers F/F09 through F/F24. Each flip-flop controls the illumination state of one display indicator lamp. The flip-flops are controlled by data input signals, display control signal, and P time signals from P0 through P15. The display control signal is applied to both input terminals of all 16 display register flip-flops, so unless the display control signal is true, all flip-flops are inhibited and cannot change configuration. Data signals carry the input data to the display register flip-flops and, if the display control signal is true, causes the display register to change configuration when the P time occurs for each display register flip-flop. Any display register flip-flop set true causes a corresponding display indicator lamp to glow, and any display register indicator lamp that glows indicates a binary 1 in that digit position.

Section II. DIGITAL DATA DISPLAY FUNCTION, DETAILED FUNCTIONAL THEORY

33. General

This section contains detailed functional theory describing the digital data display function operation in detail. The section is divided into paragraphs which describe operation of specific circuits. Paragraph 34 describes input signals supplied to the digital data display function, paragraph 35 provides the names of all flip-flops and the logic within the function, and the remaining paragraphs describe operation of the circuits in detail.

34. Input Signals

(fig. 23)

Paragraphs 34*a* and 34*b* list the input signals to the digital data display function supplied by other functions within the radar data processing center subsystem. Paragraph 34*a* lists all input signals used in logic equations of the function. Paragraph 34*b* lists all input signals supplied to the patch board on the digital data display control panel. The only output signals supplied by the digital data display function are timing signals generated by clock pulse regenerators and are routed to the tracking computer test function for digital circuit timing (fig. 23).

a. Logic Term Input Signals. The following chart lists all input signals supplied to the digital data display function which are used in logic equations. Input signals used for data display are listed in paragraph 34*b*. The signals listed in this paragraph are listed in numerical order by the signal designation within the function. Signal names and the use of the signal by the digital data display function are also listed.

Designation	Name	Use
W01 $\overline{W01}$	Sector number (OWE), received from the sector number counter in the timing function (TM 11-5840-271-30/3).	Provides sector number comparison for input data timing.
$\overline{W05}$	Major cycle units OWE, received from the storage function (TM 11-5840-271-30/3).	Supplies major cycle units coincidence for program step selection circuit.

Designation	Source	Use
W06	Major cycle tens and minor cycle OWE, received from the storage function.	Supplies major cycle tens and minor cycle coincidence for program step selection circuit.

b. Patch Board Input Signals. The following chart lists data input signals supplied to the digital data display control panel patch board by the storage function (TM 11-5840-271-30/3). The signals are listed numerically by the test point number at which they appear.

Test point	Designation	Name
1	Not used	
2	W02	M Q dump band 1 OT
3	W03	M Q dump band 1 OWE
4	W04	Result band 1 OT
5	W05	Result band 1 OWE
6	W06	M Q dump band 2 OT
7	W07	M Q dump band 2 OWE
8	W08	Result band 2 OT
9	W09	Result band 2 OWE
10	W10	M Q dump band 3 OT
11	W11	M Q dump band 3 OWE
12	W12	Result band 3 OT
13	W13	Result band 3 OWE
14	W14	$\Sigma\Delta\theta$
15	W15	$\Sigma\Delta\bar{R}$
16	W16	ΣH
17	W17	$\Sigma\Delta\phi$
18	W18	T Time
19	W19	T1 Time
20	W20	T2 Time
21	W21	θ'_p
22	W22	θ'_p OWE
23	W23	θ''_p
24	W24	θ''_p OWE
25	W25	R^1_p
26	W26	ϕ'_p
27	W27	Z_p
28	W28	R_p
29	W29	X_p
30	W30	Y_p
31	W31	X_{sm}
32	W32	Y_{sm}
33	W33	$\dot{X}$ Local
34	W34	$\dot{Y}$ Local
35	W35	ρ_p
36	W36	X_{DB}
37	W37	Y_{DB}
38	W38	h′
39	W39	Major cycle units OWE
40	W40	Major cycle tens and minor cycle OWE.
41	W41	Temporary storage band 1 OT
42	W42	Temporary storage band 1 OWE
43	W43	Temporary storage band 2
44	W44	Temporary storage band 3
45	W45	Temporary storage band 4
46	W46	Temporary storage band 5
47	W47	Action band 5 OT
48	W48	Action band 5 OWE
49	W49	Action band 6 OT
50	W50	Action band 6 OWE
51	W51	X Store
52	W52	Y Store
53	W53	Action band 1 OWE
54	W54	Action band 1 TWE
55	W55	Action band 2 OT
56	W56	Action band 2 OWE
57	W57	Manual entry band
58	W58	X Local extrapolate
59	W59	Y Local extrapolate
60	W60	X Remote extrapolate
61	W61	Y Remote extrapolate
62	W62	Velocity advance
63	W63	X ADL engagements
64	W64	Y ADL engagements
65	W65	$\dot{X}$ Remote
66	W66	$\dot{Y}$ Remote
67	W67	TN Remote OWE
68	W68	Action band 4 OT
69	W69	Action band 4 OWE
70	W70	Output buffer store
71	W71	Action band 3 OT

Test point	Designation	Name
72	$\bar{W}72$	Action band 3 OWE
73 through 100	spare test points	

35. Flip-Flop Logic

The following chart provides a list of flip-flops contained in the digital data display function. Flip-flops are listed numerically by designation with the flip-flop name and the logic equation also listed.

Designation	Name	Logic
F/F05	Start display	J05 = S01–01 (differentiated) K05 = S11–01 Q05 Q06 P0
F/F06	Input data timing	J06 = (S02–02 S03–01 S03–02 S03–03 S03–04 S03–05 S03–06 S03–07 S03–08) + (S02–01 $\bar{Q}$06 P0) K06 = (W01 G01 S02–01) + ($\bar{W}$01 G02 S02–01) + (S02–02 Q06 P0) + (S2B–01)
F/F07	Data input	J07 = $\bar{K}$07 K07 = S12–01
F/F08	Display control	J08 = Q05 Q06 P0 K08 = Q08 P0
F/F09	Display register LSD	J09 = GQ07 GQ08 P01 K09 = G$\bar{Q}$07 GQ08 P01
F/F10	Display register 2d LSD	J10 = GQ07 GQ08 P02 K10 = G$\bar{Q}$07 GQ08 P02
F/F11	Display register 3d LSD	J11 = GQ07 GQ08 P03 K11 = G$\bar{Q}$07 GQ08 P03
F/F12	Display register 4th LSD	J12 = GQ07 GQ08 P04 K12 = G$\bar{Q}$07 GQ08 P04
F/F13	Display register 5th LSD	J13 = GQ07 GQ08 P05 K13 = G$\bar{Q}$07 GQ08 P05
F/F14	Display register 6th LSD	J14 = GQ07 GQ08 P06 K14 = G$\bar{Q}$07 GQ08 P06
F/F15	Display register 7th LSD	J15 = GQ07 Q08 P07 K15 = G$\bar{Q}$07 Q08 P07
F/F16	Display register 8th LSD	J16 = GQ07 Q08 P08 K16 = G$\bar{Q}$07 GQ08 P08
F/F17	Display register 9th LSD	J17 = GQ07 Q08 P09 K17 = G$\bar{Q}$07 Q08 P09
F/F18	Display register 10th LSD	J18 = GQ07 Q08 P10 K18 = G$\bar{Q}$07 Q08 P10
F/F19	Display register 11th LSD	J19 = GQ07 Q08 P11 K19 = G$\bar{Q}$07 Q08 P11
F/F20	Display register 12th LSD	J20 = Q07 Q08 P12 K20 = $\bar{Q}$07 Q08 P12

Designation	Name	Logic
F/F21	Display register 13th LSD	J21 = Q07 Q08 P13 K21 = $\bar{Q}$07 Q08 P13
F/F22	Display register 14th LSD	J22 = Q07 Q08 P14 K22 = $\bar{Q}$07 Q08 P14
F/F23	Display register 15th LSD	J23 = Q07, GQ08 P15 K23 = $\bar{Q}$07 Q08 P15
F/F24	Display register MSD	J24 = Q07 Q08 P0 K24 = $\bar{Q}$07 Q08 P0
F/F25	Major cycle tens and minor cycle	J25 = $\bar{K}$25 K25 = $\bar{W}$06
F/F26	Major cycle units	J26 = $\bar{K}$26 K26 = $\bar{W}$05

36. Display Register Data Input Circuit

(fig. 15)

Digital input information is routed to the digital data display register through the patch board test probe S12 on the 501051 unit, level B. To obtain digital input information for display, S12 is inserted into any test point from 2 through 72 on the patch board or into any test point containing digital information on any function, receiving the same clockpulse in the RDPC sybsystem. Digital information is routed to the patch board from the memory bands in the storage function. Selection of these signals is described in paragraph 36*a*. Selecting digital information to be displayed from sources other than the patch board is described in paragraph 36*b*.

a. Data Selection From Memory Circuits. Input signals listed in paragraph 34*b* provide a source of digital information from the local memory. These signals are routed to the digit data display control panel patch board from the memory bands. The memory drum bands are each divided into 100 sectors (word slots) so that, in one rotation of the memory drum, 100 digital information words are read into a test point on the display control patch board. The digital information words contain 16 bits or digits of information. Information concerning a particular information word and the memory band sector in which the word occurs is contained in the troubleshooting procedures for most functions in the RDPC subsystem. Sector number selection is described in paragraph 38. When the test probe is inserted into a patch board test point containing digital information, all the digital information appearing at that point is routed by test probe output signal S12–01 to data input F/F07. F/F07 follows the digital information input presented through signal S12–01, and output signals Q07 and $\bar{Q}$07 represent the digital input information one bit later than presented. Q07 and $\bar{Q}$07 are routed to the display register but do not cause the display register to change configuration until the display register display control signal Q08 is set true.

b. Data Selection From Digital Circuits. Information may be read into the digital data display register from any digital circuit in the RDPC subsystem, providing the function containing the digital circuit receives the same 152 timing pulses as the digital data display function. To obtain a display of the output from any digital circuit, the patch board test probe is connected to any test point where the information occurs. The test probe is connected to the digital circuit $\bar{Q}$ output or equivalent to maintain the correct relationship between the received information and the display register indicator lamps. All digital information occurring at the selected test point is read into data input F/F07. F/F07 follows the digital information presented by patch board test probe output signal S12–01. F/F07 output signals Q07 and $\bar{Q}$07 represent the digital information, and are routed to the display register; however, they do not cause the display register to change configuration until data control signal Q08 is set true. Timing signals providing the desired display are patched into the SPECIAL GATE test jacks A1 through A8 and are used to control the timing which sets data control

signal Q08 true. The specil gate timing circuit is described in paragraph 39.

37. Timing Circuit Selection

(fig. 16)

Timing circuit selection is provided through DISPLAY GATE TIMING switch S02. S02, a double-pole double-throw type switch, provides output signals S02–01 and S02–02. Output signal S02–01 is true when the SN position is selected and signal S02–02 is true when the SPECIAL position is selected. These signals are used in the logic equations for input data timing F/F06 so that only the selected timing circuit will affect the state of F/F06. When S02 is placed in the SN position, timing for digital information input from the patch board is provided through selection of the memory band sector where the information occurs. Sector number selection is described in paragraph 38. To provide timing for input information from other digital circuits, the DISPLAY GATE TIMING switch is placed at the SPECIAL position and timing signals are patched in through the special gate. Timing through the special gate is described in paragraph 39.

38. Sector Number Selection Circuit

(fig. 17)

The sector number selection circuit provides input data timing for digital information displayed by the digital data display register. The circuit allows selection of a specific memory band sector containing a 16 digit information word, and the circuit output is used in the logic equations of input data timing F/F06 so that F/F06 is set false at P0 until the selected sector occurs. Each sector consists of one information word (16 digits) on each of the 63 memory bands and information concerned with any one track operation is contained within one sector of the memory. By selecting a particular sector, the information contained in the selected sector of all memory bands is checked. The sector number selection circuit operation is described in paragraphs 38*a* and 38*b*.

a. Sector Number Selection. Each of the 100 sectors on the drum are selected by operation of the seven SN SELECT switches on the digital display function control panel. Each of the seven switches represents one digit of a seven digit binary word. A binary 1 is represented by a switch in the up position, and a binary 0 is represented by a switch in the down position. Any drum sector is selected by operating the switches to represent the desired SN in binary code. The sector number LSD is represented by S04 which is the switch on the right and the MSD is represented by S10 which is the switch on the left. An example of SN SELECT switch setting is provided in paragraph 30*a*. The following chart provides a complete listing of SN SELECT switch settings for all memory drum sectors.

Sector numbers	1	2	3	4	5	6	7	8	9	10
1–10	0000001	0000010	0000011	0000100	0000101	0000110	0000111	0001000	0001001	0001010
11–20	0001011	0001100	0001101	0001110	0001111	0010000	0010001	0010010	0010011	0010100
21–30	0010101	0010110	0010111	0011000	0011001	0011010	0011011	0011100	0011101	0011110
31–40	0011111	0100000	0100001	0100010	0100011	0100100	0100101	0100110	0100111	0101000
41–50	0101001	0101010	0101011	0101100	0101101	0101110	0101111	0110000	0110001	0110010
51–60	0110011	0110100	0110101	0110110	0110111	0111000	0111001	0111010	0111011	0111100
61–70	0111101	0111110	0111111	1000000	1000001	1000010	1000011	1000100	1000101	1000110
71–80	1000111	1001000	1001001	1001010	1001011	1001100	1001101	1001110	1001111	1010000
81–90	1010001	1010010	1010011	1010100	1010101	1010110	1010111	1011000	1011001	1011010
91–100	1011011	1011100	1011101	1011110	1011111	1100000	1100001	1100010	1100011	1100100

b. Sector Timing. Sector timing is provided by DISPLAY GATE TIMING switch S02, SN SELECT switches S04 through S10, and input data timing F/F06 (fig. 17). The following equations show the portion of F/F06 logic used during SN selection.

$$J06\ (\text{partial}) = (S02\text{–}01\ P0\ \bar{Q}06) + \ldots.$$

$$K06\ (\text{partial}) = (W01\ G01\ S02\text{–}01) + (\bar{W}01\ G02\ S02\text{–}01) + \ldots.$$

With DISPLAY GATE TIMING switch S02 in the SN position, true logic occurs at the J input of

F/F06 at P0 time of each sector and output Q06 is set true one P time later at P01. However, true logic occurs at the K input of F/F06 at some P time between P09 and P15 which sets the flip-flop false. This prevents Q06 from being true during P0 time of any sector until SN number coincidence occurs. Q06 must be true during P0 time to effect a change in the display register.

(1) *Logic terms G01 and G02.* Logic terms G01 and G02 are developed as a result of the SN SELECT switch positioning. The switches are designated S04 through S10 and each switch provides two output signals. The −01 output signal from each switch is true when the switch is in the down position and the −02 signal is true when the switch is in the up position. G01 signal is generated from a coincidence between S04–01 through S10–01 and P09 through P15 respectively. G02 signal is generated from a coincidence between S04–02 through S10–02 and P09 through P15 respectively. All of the anded −01 signals are combined in an or gate and routed to gate amplifier G01 and all the −02 signals are combined in a separate or gate and routed to gate amplifier G02. The logic for G01 and G02 is as follows:

G01 = (S04–01 P09)
+ (S05–01 P10)
+ (S06–01 P11)
+ (S07–01 P12)
+ (S08–01 P13)
+ (S09–01 P14)
+ (S10–01 P15)

G02 = (S04–02 P09)
+ (S05–02 P10)
+ (S06–02 P11)
+ (S07–02 P12)
+ (S08–02 P13)
+ (S09–02 P14)
+ (S10–02 P15)

Term G02 is the selected sector number from P09 to P15 and term G01 is the complement of G02, for the time interval P09 to P15.

(2) *Logic terms W01 and $\overline{W}$01.* Logic term W01 is the SN OWE signal supplied by the timing function and logic term $\overline{W}$01 is the complement of W01. In the K input logic of F/F06, W01 is anded with G01 which is the complement of the selected SN from P09 through P15 and is the complement of W01 during the same time. $\overline{W}$01 is anded with G02 which is the selected SN and they are also complements. Under these conditions, either the W01 G01 or the $\overline{W}$01 G02 combination is true for at least one P time between P09 and P15 during every sector until sector coincidence occurs. When the SN OWE signal is the same as the selected SN, neither combination is true and input data timing flip-flop F/F06 remains true through P0 of the selected sector.

39. Special Gate Timing Circuit

(fig. 16)

The special gate timing circuit provides input data timing for information received from digital circuits other than the memory bands. The circuit contains SPECIAL GATE input test jacks A1 through A8 on the digital data display control panel, DISPLAY GATE TIMING switch S02, and input data timing F/F06. The following equations show the portion of F/F06 logic used during special gate timing.

J06 (partial) = (S02–02 S03–01 S03–02 S03–03 S03–04 S03–05 S03–06 S03–07 S03–08) + . . .

K06 (partial) = (Q06 P0 S02–02) + . . .

With the DISPLAY GATE TIMING switch placed in the SPECIAL position, a true state occurs at the K input of F/F06 at P0 time of each sector. This condition sets the F/F06 output signal Q06 false and the signal remains false until a true state occurs at the J input of F/F06. Q06 must be true during P0 to effect a change in the display register. J input logic for F/F06 is provided by SPECIAL GATE output signals S03–01 through S03–08 which are routed from input test jacks A1 through A8 respectively. Timing conditions which set the J input logic true, at least one P time prior to P0 of the word time to be displayed, is patched into the SPECIAL GATE test jack. Any number of different signals between 1 and 8 are connected to separate SPECIAL GATE test jacks to provide input data timing. All signals connected to the test jacks must be true for at least one P time between P01 and P15 OWE and at least one signal must be false at all other times. The signals to be connected into the

eight SPECIAL GATE test jacks depend upon the desired display conditions. For example: the detailed functional theory of any function may state that a particular flip-flop is true from P05 through P09 when A, B, and C are true. Signals representing A, B, and C are then patched into the special gate along with a P time signal between P01 and P15 OWE. The A, B, and C signals represent the display conditions, and the P time is the time prior to P0 when F/F06 is to be set true. When the selected display conditions occur at the proper P time, a true state is present at the J input of F/F06 and the flip-flop is set true. Output signal Q06 goes true one P time later and remains true until P01 of the selected word time. Since F/F06 must only be true during P0 of the selected word time to provide a display condition, the digital information from the flip-flop being checked enters the display register.

40. Program Step Selection Circuit

(fig. 18)

Program step selection provides an additional input data timing signal which prevents F/F06 from going true during P0 except when a selected major cycle or a minor cycle occurs. Program steps are selected by operating MAJOR UNITS switch S1, MAJOR TENS switch S2, and MINOR switch S3, located on the TCC STEP SELECTOR panel in the 501056 unit. These switches are operated in combination to select any major cycle from 1 through 68 and any minor cycle from 1 through 13 of the selected major cycle. When a major cycle and minor cycle are selected, the program step selector output signal S2B–01 is true during every word time until one word time prior to the selected cycle. Output S2B–01 is routed to the K input of input data timing F/F06, and sets F/F06 false OWE until the selected cycle occurs. The program step selection circuit logic is as follows:

$$\begin{aligned} \text{S2B–01} = &(\text{S1–01 } \bar{Q}26) \\ &+(\text{S2A–01 } \bar{Q}25) \\ &+(\text{S3A–01 P52}) \\ &+(\text{S3B–01 P13}) \\ &+(\text{S3C–01 P14}) \\ &+(\text{S3D–01 P15}) \end{aligned}$$

The program step selection circuit is used in conjunction with the sector number selection circuit and the special gate timing circuit may or may not be used depending upon the timing necessary to obtain a particular display. If the program step selector circuit is not being used, the MAJOR TENS switch S2 is rotated fully counterclockwise. This operation opens the output signal circuit so that S2B–01 does not effect F/F06. Since the major cycle selection occurs one word early, program step selection cannot be used when one word early signals are being displayed.

a. Major Cycle Selection. To provide major cycle selection, major cycle units OWE signal $\bar{W}05$ and major cycle tens OWE signal $\bar{W}06$ are routed to the program step selection circuit from the storage function. Signal $\bar{W}05$ is then routed to the K input of major cycle units F/F26 and $\bar{W}06$ is routed to the K input of major cycle tens and minor cycle F/F25. F/F25 and F/F26 are K$\bar{K}$ flip-flops, the output signals follow the input signal applied to the K input. Output signal $\bar{Q}26$ is routed to an and gate and is anded with a P time signal from P01 through P10 depending upon the position of major cycle units select switch S1. P times P01 through P10 are applied to the S1 switch contacts so that the P time routed to the major cycle units and gate depends upon the switch position. Output signal $\bar{Q}25$ is also routed to an and gate where it is anded with a P time signal from P01 through P07 depending upon the position of major cycle tens select switch S2A. P times P01 through P07 are applied to the S2A switch contacts so that the P time routed to the major cycle tens and gate depends upon the switch position. The output signals from the tens and gate and the units and gate are combined in an or gate and the combined signal is then routed to switch S2B. Either the tens and gate, the units and gate, or both gates are set true for at least one P time every word time until one word time prior to the selected major cycle. Switch S2B and switch S2A are mechanically connected so that when any major cycle between 01 and 68 is selected, the true signal from either and gate passes through the contacts of switch S2B and is routed to the K input of F/F06. F/F06 is set false by signal S2B–01 each word time at the P time selected by switches S1 and S2A. When the selected major cycle does occur OWE, no P time between P01 and P10 will coincide with a true $\bar{Q}26$ or $\bar{Q}25$ signal and neither and gate is true. Signal S2B–01 is not set true and F/F06 remains true until the next word time.

b. Minor Cycle Selection. Minor cycles occur one cycle every DREV for 13 DREVs during certain

major cycles. Operations occur during minor cycles and these operations can be checked at any minor cycle using the program step selector circuit. A major cycle at which the minor cycle 13 DREV operation occurs is selected first and the minor cycle is then selected on MINOR switch S3. S3 is a four wafer rotary switch with major cycle tens and minor cycle flip-flop output signals Q25 and $\bar{Q}25$ connected to the switch contacts of each wafer. Each wafer selects either the Q25 or $\bar{Q}25$ signal depending upon the switch position and each wafer provides one output signal which is applied to an, and gate. When S3 is set to positions 1 through 12 the Q25 and $\bar{Q}25$ signals applied to the four and gates represent a four digit binary word from 0 through 11 respectively. Each of the four output signals is anded with a P time between P12 and P15 and the anded signals are then combined in an or gate and routed to the contacts of switch S2B. During every word time of the 13 DREV operation until the selected minor cycle occurs, at least one anded term is true. This true signal is routed through the contacts of switch S2B to the K input of F/F06. When the selected minor cycle does occur, P12 through P15 do not coincide with a true Q25 or $\bar{Q}25$ signal and F/F06 remains true until the next word time.

41. Display Register Control

(fig. 19)

Display register control provides input data timing for the digital data display register so that the display register only changes configuration during preselected intervals. Selected test information is applied to the display register through the data input circuits, but this information cannot cause the display register to change configuration until all conditions of the display register control are met. The display register control consists of the input data timing circuit, start display circuit, and the display control circuit.

a. Input Data Timing Circuit. Input data timing is provided by input data timing F/F06. Logic for F/F06 is provided by timing circuit selection, sector number selection, special gate timing, and program step selection circuits which are described in paragraphs 37 through 40. These circuits provide timing conditions for F/F06 to prevent output signal Q06 from going true during P0 of any word until timing coincidence occurs. Q26 is routed to display control F/F08 and is used in the logic equation which sets F/F08 true.

b. Start Display Circuit. The start display circuit consists of START DISPLAY pushbutton S01, CONTINUOUS HOLD switch S11, and start display F/F05. When depressed, S01 provides a false output signal which is applied to the J′ input of F/F05, and the flip-flop is set true immediately. Output signal Q05 is routed to display control F/F08, and must be true to change the display register configuration. The CONTINUOUS HOLD switch S11 output signal S11–01 is routed to the K input of F/F05 so that when the switch is placed in the START OR STOP position, S11–01 is true and Q05 is set false at P01 time after Q05 and Q06 become true at P0. This condition prevents display control F/F08 from going true again after the first word has entered the display register and the display register holds the configuration set by the first word. The logic equations for F/F05 are—

$$J05 = S01\text{–}01 \text{ (differentiated)}$$
$$K05 = S11\text{–}01\ Q05\ Q06\ P0$$

If the CONTINUOUS HOLD switch S11 is placed in the CONTINUOUS position, S11–01 is false and when S01 is depressed flip-flop F/F05 goes true and remains true indefinitely.

c. Display Control Circuit. The display control circuit consists of start display F/F05, input data timing F/F06, and display control F/F08. The logic equations for F/F08 are:

$$J08 = Q05\ Q06\ P0$$
$$K08 = Q08\ P0$$

To set display control F/F08 true, F/F05 and F/F06 must be true at P0. F/F06 is only true at P0 during timing coincidence for the particular signal input. When all connections have been made, switches set, and the START DISPLAY pushbutton S01 is depressed, F/F05 is set true. When Q05 and Q06 are both true at P0, display control F/F08 is set true and the output signal Q08 goes true one P time later at P01. Due to the logic on the K input of F/F08, the flip-flop remains true for one word time from P01 0T to P0 one word later (OWL). This logic permits only the selected binary word to enter the display register at the timing intervals selected by Q05 and Q06. Q08 is routed to the display register to provide control of the digital information being entered.

42. Display Register

(fig. 20)

The display register provides a visual display of any binary word containing 16 digits or less. Each digit of the binary word is represented by one of 16 indicator lamps located on the digital data display control panel. The indicator lamps are arraged so that each digit of the binary word entered affects only the lamp appearing in the same digit position between P0 and P15. Each indicator lamp is controlled by one of 16 display register flip-flops. The logic for display registers F/F09 through F/F24 is listed in paragraph 35. Each display register flip-flop receives the data control signal which is routed to both the J and K inputs of all 16 display register flip-flops as either Q08 or gate amplified GQ08. GQ08 and Q08 are false at all times until the selected control conditions exist and are set true for one word time from P01 0T to P0 OWL. This prevents any display register flip-flop from changing configuration except during the selected word time. The data input flip-flop output signals are also routed to the display register flip-flops as either Q07, $\overline{Q}$07 or gate amplified GQ07, G$\overline{Q}$07. Data input signal Q07 or gated signal GQ07 are routed to the J inputs of all display register flip-flops and $\overline{Q}$07 or G$\overline{Q}$07 is routed to the K inputs of all display register flip-flops. While the patch board test probe is connected to a digital input data source, the data input signals are changing states constantly as the source changes states; however, these signals cannot cause any flip-flop to change configuration until the data control signal goes true. Timing for the display register flip-flops is supplied by P time signals from P0 through P15. Each P time is routed to the J and K inputs of one display register flip-flop, so the flip-flop can only change states during the applied P time. When the data control signal is true, each display register flip-flop changes configuration according to whether the Q07 or $\overline{Q}$07 signal is true when the associated P time occurs. The associated P times for F/F09 through F/F24 occur from P01 0T to P0 OWL respectively. The $\overline{Q}$ output signals from the display register flip-flops are each routed to one display indicator lamp. $\overline{Q}$ output signals are used to supply a -6 volt signal which causes the indicator lamp to glow when the flip-flop Q output is set true. When any digital display indicator lamp glows a binary 1 is indicated that digit position and a binary 0 is indicated in a digit position where the lamp does not glow.

CHAPTER 4
GENERAL TROUBLESHOOTING INFORMATION

43. General

Troubleshooting procedures described in this volume are concerned with malfunctions in operation of the tracking computer test and digital data display functions and do not include procedures for troubleshooting other RDPC subsystem functions. Information contained in chapters 4, 5, and 6 of this volume aids repairmen in detecting abnormal operation and in determining the cause of malfunctions occurring in the circuits of the tracking computer test function and the digital data display function. This chapter provides general troubleshooting information applicable to both functions. Chapter 5 provides troubleshooting information for the tracking computer test function and chapter 6 provides troubleshooting information for the digital data display function.

44. Troubleshooting Procedure

The troubleshooting procedures contained in chapters 4 and 5 are divided into three sections. Section I of each chapter contains a preliminary procedure, section II contains an operational test, and section III contains circuit troubleshooting procedures.

a. Prelimnary iprocedures are performed to establish the state of the equipment prior to troubleshooting. These instructions are also referenced in the troubleshooting procedures in order to return all switches on the function tested to a neutral position or common starting point.

b. Operational tests are used to examine a function to determine whether a malfunction exists, and also to isolate a malfunction to a circuit group. Circuit groups are referenced by name and paragraph number in the remarks column of the operational test to provide a guide to the proper circuit troubleshooting procedure. When a malfunction is detected during an operational test, the referenced troubleshooting procedure is performed to isolate the malfunction. Corrective action is then taken and the operational test is repeated to determine if any further malfunctions exist.

c. Circuit troubleshooting procedures are a step-by-step trouble isolation program for a circuit group within a function. The troubleshooting procedures for each circuit group are contained in a separate paragraph, and are referenced from the operational test, so that the number of steps required to locate and isolate a malfunction is minimized.

45. Troubleshooting Data

Troubleshooting information contained in this volume is presented as a guide to aid repairmen in localizing malfunctions of the tracking computer test and digital data display functions. Power requirements and timing pulses for the functions are not discussed in these troubleshooting procedures; however, test points for both the power and timing pulse inputs are shown on the detailed functional diagram (fig. 22 and 23). Troubleshooting of the power distribution is contained in TM 11-5840-271-30/18 and troubleshooting of the timing signals is contained in TM 11-5840-271-30/3. Shorted or broken wiring is best located through point-to-point resistance and continuity measurements using the appropriate detailed functional diagram. The computer test function detailed functional diagram (fig. 22) and digital data display function detailed functional diagram (fig. 23) show the logic of each circuit as well as the signal flow and basic circuit content, and provide the best means of following the step-by-step troubleshooting procedure through a particular circuit. Circuit block diagrams are also useful during circuit troubleshooting procedures and are referenced where applicable. Test points shown on the detailed functional diagrams are located on the front panel of the unit in which they are shown. Additional test points are provided on each of the flip-flop card assemblies. When these test points are listed in the troubleshooting procedures,

they are followed by the card assembly slot number.

a. The circuits of the tracking computer test and digital data display functions are used for troubleshooting other functions contained in the RDPC subsystem. Since most of the tracking computer test and digital data display function circuits are not used during RDPC subsystem operation, shooting of these circuits can be accomplished without interfering with the subsystem operation. However, subsystem operation is effected by the clear memory and computer mode selection circuits of the tracking computer test function. Do not operate these two circuits during the troubleshooting procedures unless specificially instructed.

b. True and false indications are referred to during the troubleshooting procedures. The true state is 0v or dc ground and the false state is −6v dc.

46. Test Equipment Required

The following three items of test equipment and their accessories are supplied with the RDPC subsystem, and are used during the computer test and digital data display functions troubleshooting procedures.

Equipment	Use
Test set, 501039	Used to check the three test band slot counter flip-flop card assemblies.
Multimeter, AN/URM–105.	Used to make voltage and resistance measurements.
Oscilloscope, AN/USM–81	Used for signal tracing by waveform observation.

CHAPTER 5
TRACKING COMPUTER TEST FUNCTION TROUBLESHOOTING

Section I. PRELIMINARY PROCEDURE

47. General

This section contains the procedure for equipment setup and initial switch operations for the computer test function. This procedure is accomplished before performing the operational test contained in section II. The circuit troubleshooting procedures contained in section III also use this procedure. This procedure establishes the state of the equipment prior to test, and prevents unnecessary repetition of switch settings and abnormal indications because of incorrect switch settings. All switches and indicators listed in sections I, II, and III are located on the computer test set and display control 501051 unit, level A. Instructions in paragraph 49 of this section are referred to during the test procedures in order to return all switches to a neutral or common starting position.

48. Equipment Setup

a. Pull out unit drawer 501051 to provide access to the computer test function control panel, level A. Pull out unit drawer 501056 to provide access to the flip-flop card assembly test points.

b. Set up oscilloscope AN/USM-81 as per TM 11-6625-219-12.

c. Check that power is supplied to the tracking computer test function.

49. Initial Switch Operation

The following chart lists the computer test function switches and the operation which positions each switch at a neutral or common starting position.

Step	Switch name	Switch No.	Operation
1	SLOT SEL LSD	S18	Operate ccw to 0 position.
2	SLOT SEL MSD	S19	Operate ccw to 0 position.
3	INFORMATION INPUT	S2 through S17	Operate all 16 switches to the down position.
4	INFO SELECTOR	S20	Operate to TEST position.
5	MAJOR CYCLE SEL UNITS	S32	Operate ccw to 0 position.
6	MAJOR CYCLE SEL TENS	S33	Operate ccw to 0 position.
7	ONCE ONLY-EVERY DREV	S24	Operate to EVERY DREV position.
8	MAN MODE	S27	Switches S27 and S28 are normally set at the OPERATIVE position; however, since operation of the tracking computer is involved, do not change the position of these switches until required to do so in specific test instructions.
9	AUTO MODE	S28	
10	ENTER INFO	S1	These pushbutton switches are listed here for reference purposes. Press these switches only when required to do so by specific instruction.
11	START COMPUTATION	S26	
12	MEMORY CLEAR (located on front panel of 501051 unit).	S30	

Section II. OPERATIONAL TEST

50. General

This section contains a complete operational test procedure which is used to determine whether a malfunction exists in the tracking computer test function circuits. Each step of the procedure is performed sequentially unless an abnormal indication is obtained. The repairman can isolate an indicated malfunction by using the circuit troubleshooting procedure referenced in the remarks column of the operational test. After the repair action is taken, the operational test procedure is repeated from the beginning to determine whether any further malfunctions exist.

51. Operational Test Procedure

(fig. 22)

The following chart lists the complete operational test procedure for the tracking computer test function. Chapter 4 must be read prior to performing this test procedure. Oscilloscope AN/USM-81 is used extensively throughout this test and is connected as listed in the test point and sync source columns. The test points listed in both columns are located on the 501051 unit unless otherwise specified. Paragraph numbers appearing in the remarks column refer to the circuit troubleshooting procedure used to isolate a malfunction. Read all instructions pertaining to each step prior to making oscilloscope connections or performing the listed procedures. All pulse width and repetition rate indications are listed as approximate values.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
1	Perform initial switch operation (par. 49). Operate SLOT SEL LSD switch S18 and SLOT SEL MSD S19 successively through each octal position from 1 to 37.	TP5, slot J16C, 501056 unit.	int	100 microsecond pulse reoccurring every 3.3 milliseconds at each selected switch position.	Checks test band slot selection circuit operation. If indication is abnormal, see paragraph 53.
2	Operate SLOT SEL LSD switch S18 to position 1 and SLOT SEL MSD switch S19 to position 0. Operate INFORMATION INPUT P0, P03, P06, P09, P12, and P15 switches S2, S5, S8, S11, S14, and S17 to the up position. Press ENTER INFO switch S1.	TP1C	int	16 bit word 0110110110110110 (complement of INFORMATION INPUT switch positions), 100 microseconds in duration and the word reoccurs every 3.3 milliseconds.	Checks information entry circuit operation. If indication is abnormal, see paragraph 54.
3	Same as step 2	TP1B and TP2B	int	100 microsecond pulse reoccurring every 3.3 milliseconds at each test point.	Checks data display control circuit with INFO SELECTOR switch S20 at the TEST position. If indication is abnormal, see paragraph 55.
4	Same as step 2	TP35C	int	16 bit word 1001001001001001 (same as INFORMATION INPUT switch positions).	Checks part of display data entry circuit. If indication is abnormal, see paragraph 56.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
5	Same as step 2	TP38C	int	16 bit word 0110110110110110 (complement of INFORMATION INPUT switch positions).	Checks part of display data entry circuit. If indication is abnormal, see paragraph 56.
6	Operate INFORMATION INPUT P0 through P15 switches S2 through S17 to the up position. Press ENTER INFO switch S1.	None	None	DISPLAY REGISTER P0 through P15 indicators glow.	Checks part of display register circuit. If indication is abnormal, see paragraph 57.
7	Operate INFORMATION INPUT P0 through P15 switches S2 through S17 to the down position. Press ENTER INFO switch S1.	None	None	DISPLAY REGISTER P0 through P15 indicators extinguish.	Checks part of display register circuit. If indication is abnormal, see paragraph 57.
8	Operate SLOT SEL LSD switch S18 to position 0, and SLOT SEL MSD switch S19 to position 2. Operate INFORMATION INPUT P04, P05, P07, P08, P10, and P11 switches S6, S7, S9, S10, S12, S13 to the up position. Press ENTER INFO switch S1.	None	None	DISPLAY REGISTER P04, P05, P07, P08, P10, and P11 indicator lamps glow to indicate word entered on test band.	Steps 8 and 9 enter a known test word and a major cycle constant into test band slots 20 and 37, respectively. The tracking computer then provides a major cycle count during the test sector which is used for checking the display data entry and data control circuits. If indications are abnormal, check initial switch operations (par. 49) and

					then repeat steps 8 and 9.
9	Operate SLOT SEL LSD switch S18 to position 7, and SLOT SEL MSD switch S19 to position 3. Operate INFORMATION INPUT P0 and P01 switches S2 and S3 to the up position and P02 through P15 switches S4 through S17 to the down position. Press ENTER INFO switches S1.	None	None	DISPLAY REGISTER P0 and P01 indicator lamps glow to indicate word entered on test band. (0000000000000011).	
10	Operate INFO SELECTOR switch S20 to the PATCH position Operate ONCE ONLY-EVERY DREV switch S24 to the ONCE ONLY position. Press START COMPUTATION switch S26.	TP8, slot J2C, 501056 unit.	int	False for 100 microseconds every 10 milliseconds. Three minutes after S26 is pressed, indicator goes thru and remains true.	Partially checks the major cycle selection circuit. If indication is abnormal, see paragraph 55.
11	Operate MAJOR CYCLE SEL UNITS switch to position 1. Press START COMPUTATION switch S26.	TP8, slot J2C, 501056 unit.	int	False for 100 microseconds every 10 milliseconds except during major cycle 1. MC1 repeats at least once every 6 seconds.	Partially checks major cycle selection circuit. If indication is abnormal, see paragraph 54.
12	Insert patch board test probe S25 into test jack 70 on computer test control panel.	None	None	DISPLAY REGISTER indicator lamps P04, P05, P07, P08, P10, and P11 glow to	Checks display data control and data entry circuits. If indication is abnormal, see

Step	Procedure	Test point	Sync source	Normal indication	Remarks
	Operate MAJOR CYCLE SEL UNITS switch S32 to position 4 and MAJOR CYCLE SEL TENS switch S33 to position 3. Press START COMPUTATION switch S26. *Note.* Steps 13 and 14 assume that the MAN MODE switch S27 and the AUTO MODE switch S28 are both in the OPERATIVE position, if any other conditions exist, both switches may be operated to the OPERATIVE position momentarily and then returned to the previously set position.			indicate received information word.	paragraph 55. And if malfunction is not located, see paragraph 56. *Note.* CLEAR MEMORY switch S30 is not checked during this procedure because of possible interference with local track operations. S30 is checked during the subsystem maintenance checks, TM 11-5840-271-30/18.
13	None required	None	None	MAN MODE and AUTO MODE indicator lamps glow steadily when S27 and S28 are in the OPERATIVE position.	Checks MAN MODE and AUTO MODE indicator lamps. Output signals from S27 and S28 are checked during subsystem maintenance checks, TM 11-5840-271-30/18.
14	Operate AUTO MODE switch S28 to the INOPERATIVE position and return to the OPERATIVE position.	None	None	REJECT ARDME DATA indicator malp glows intermittently to indicate ARDME data is being rejected by the computer when S28 is at INOPERATIVE position.	Checks REJECT ARDME DATA circuit. If indication is abnormal, see paragraph 58.

Section III. COMPUTER TEST FUNCTION CIRCUIT TROUBLESHOOTING

52. General

This section contains circuit troubleshooting procedures which aid the repairman to isolate the malfunctions of the computer test function circuits to a card assembly or subassembly. Each circuit troubleshooting procedure is presented in a separate paragraph. The paragraphs are each referenced from the operational test in section II, so it is assumed in all procedures that a malfunction is known to exist. The oscilloscope is used extensively in all circuit troubleshooting, and is connected as indicated in the test point and sync source columns. A multimeter may be used for steady state indications as indicated in the sync source column. All pulse width and repetition rate indications are listed as approximate values. Read all instructions pertaining to each step before performing operations listed in the procedure column. Perform all step procedures sequentially unless instructions in remarks column specify otherwise.

53. Test Band Slot Selection Circuit Troubleshooting

(fig. 5 and 22)

The following chart provides the troubleshooting procedure for the test band slot selection circuit. Steps 1 through 14 check the slot coincidence, slot selection, and test band slot counter circuits and steps 15 through 20 check the test band slot counter output signals supplied to other functions. Test points referenced in this procedure are located on the 501051 unit unless otherwise specified.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
1	Perform initial switch operations (par. 49).	TP29B	−ext P13 at TP28B.	6.6 microsecond pulse	Checks presence of P14 for counter gating.
2	Operate SLOT SEL LSD switch S18 to position 1.	TP5, slot J16C, 501056 unit.	int	Slot coincidence signal Q10 for test band slot No. 1. True for 100 microseconds every 3.3 milliseconds.	Adjust oscilloscope for 3.3 milliseconds horizontal sweep. Q10 signal to appear at extreme left side of display. If indication is abnormal, proceed to step 3.
2*a*	Operate SLOT SEL LSD and SLOT SEL MSD switches S18 and S19 successively to each of the remaining 36 octal positions.	Same as step 2	Same as step 2	Q10 moves progressively across display as each position is selected (fig. 23).	With octal state 37 selected, Q10 appears at extreme right side side of display. If indication is abnormal, proceed to step 3.
2*b*	Operate SLOT SEL LSD and SLOT SEL MSD switches S18 and S19 to 0 position.	Same as step 2	Same as step 2	No slot coincidence signal.	Steps 2 through 2*b* check the complete slot selection circuit. If indications are normal, proceed to step 15. If indications are abnormal, proceed to step 3.
3	Operate SLOT SEL LSD switch S18 to position 1.	TP1, slot J16C, 501056 unit.	+ext P15 at TP30B.	J10 signal true for 100 microseconds of 3.3 millisecond sweep.	Checks F/F10, slot J16C, 501056 unit. If indication is abnormal, proceed to step 4.
4	Operate SLOT SEL LSD switch S18 successively to each position from 0 through 7 and return to 0 position.	TP27C, 501056 unit.	Same as step 3	Approximates LSD waveform at positions 1, 3, 5, and 7, and complement of LSD waveform at positions 0, 2, 4, and 6 (fig. 21).	Checks S18–01 logic at slot J15C, 501056 unit. If indication is abnormal, proceed to step 9.
5	Same as step 4	TP28C, 501056 unit.	Same as step 3	Approximates second LSD waveform at	Checks S18–02 logic at slot J15C, 501056

				positions 2, 3, 6, and 7, and complement of second LSD at positions 0, 1, 4, and 5 (fig. 21).	unit. If indication is abnormal, proceed to step 10.
6	Same as step 4	TP29C, 501056 unit.	Same as step 3	Approximates third LSD waveform at positions 4, 5, 6, and 7, and complement of third LSD at positions 0, 1, 2, and 3 (fig. 21).	Checks S18–03 logic at slot J15C, 501056 unit. If indication is abnormal, proceed to step 11.
7	Operate SLOT SEL MSD switch S19 successively to each position from 0 through 3 and return to 0 position.	TP31C, 501056 unit.	+ext P15 at TP30B.	Approximates fourth LSD waveform at positions 0 and 2, and complement of fourth LSD at positions 1 and 3 (fig. 21).	Checks S19–02 logic at slot J15C, 501056 unit. If indication is abnormal, proceed to step 12.
8	Same as step 7	TP30C, 501056 unit.	Same as step 7	Approximates MSD waveform at positions 2 and 3, and complement of MSD at positions 0 and 1 (fig.21).	Checks S19–01 logic at slot J15C, 501056 unit. If indication is abnormal, proceed to step 13.
9	None	TP5, slot J19C	Same as step 7	Approximates LSD waveform (fig. 21).	Checks SLOT SEL LSD switch S18A. If indication is abnormal, proceed to step 14.
10	None	TP5, slot J16C	Same as step 7	Approximates second LSD waveform (fig. 21).	Checks SLOT SEL LSD switch S18B. If indication is abnormal, proceed to step 14.
11	None	TP8, slot J19C	Same as step 7	Approximates third LSD waveform (fig. 21).	Checks SLOT SEL LSD switch S18C. If indication is abnormal, proceed to step 14.
12	None	TP5, slot J17C	+ext P15 at TP30B.	Approximates fourth LSD waveform (fig. 21).	Checks SLOT SEL MSD switch S19. If indication is abnormal, proceed to step 14.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
13	None	TP8, slot J17C	Same as step 12	Approximates MSD waveform (fig. 21).	Checks SLOT SEL MSD switch S19. If indication is abnormal, proceed to step 14.
14	See remarks column *Note.* The remaining steps of this procedure check the test band slot counter outputs supplies to other functions. See figure 22, sheet 3 of 3.				Test band slot counter flip-flops, F/F05 through F/F09, are each interdependent. Therefore, each flip-flop is removed and checked using the digital element test set 501039 (TM 11-6625-430-12). Check matrix cards at slots J15C and J18C if flip-flops test satisfactorily.
15	None	TP16A, TP17A, TP18A, TP19A, TP20A, and TP21A.	+ext P15 at TP30B.	Approximates LSD waveform at TP16A, TP17A, and TP18A, and complement of LSD at TP19A, TP20A, and TP21A (fig. 21).	Checks test band slot counter LSD gate amplifier outputs. If indication is abnormal, proceed to step 20.
16	None	TP25A, TP26A, TP27A, and TP29A on 501051 unit, and TP21C and TP24C on 501056 unit.	Same as step 15	Approximates second LSD waveform at TP25A, TP26A, and TP27A, and complement of second LSD at TP29A, TP21C, and TP24C (fig. 21).	Checks test band slot counter second LSD gate amplifier outputs. If indications is abnormal, proceed to step 20.
17	None	TP31A, TP35A, TP36A, and TP37A on 501051 unit, and	Same as step 15	Approximates third LSD waveform at TP31A, TP22C, and TP25C, and comple-	Checks test band slot counter third LSD gate amplifier outputs. If indication is abnormal,

		TP22C and TP25C on 501056 unit.		ment of third LSD at TP35A, TP36A, and TP37A (fig. 21).	proceed to step 20.
18	None	TP27C, TP28C, TP29C, and TP30C on 501051 unit, and TP23C and TP26C on 501056 unit.	Same as step 15	Approximates fourth LSD waveform at TP28C, TP29C, and and TP30C, and complement of fourth LSD at TP27C, TP23C, and TP26C (fig. 21).	Checks test band slot counter fourth LSD gate amplifier outputs. If indication is abnormal, proceed to step 20.
19	None	TP31C, TP32C, TP33C, TP34C, TP36C, and TP37C.	+ext P15 at TP30B.	Approximates MSD waveform at TB31C, TP36C, and TP37C, and complement of MSD at TP32C, TP33C, and TP34C (fig. 21).	Checks test band slot counter MSD gate amplifier outputs. If indication is abnormal, proceed to step 20.
20	See remarks column				When any test band slot counter gate amplifier output is abnormal, immediately check input to gate amplifier at test points shown on figure 22, sheet 3 of 3. If indication is abnormal at input to gate amplifier, check matrix card which supplies the input.

54. Test Information Entry Circuit Troubleshooting

(fig. 6 and 22)

The following chart provides the troubleshooting procedure for the test information entry circuits. Test points referenced in this procedure are located on the 501051 unit unless otherwise specified.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
1	Perform intial switch operations (par. 49).	TP15B–TP30B successively.	—ext P15 and P0–P14 at TP30B and TP15B–TP29B successively.	6.6 microsecond pulse	Checks presence of P times P0–P15 when each input P time is synchronized with previously occurring P time.
2	Operate INFORMATION INPUT P0–P15 switches S2–S17 to the up position.	TP6C–TP21C successively.	int or use multimeter AN/URM–105.	False	Each test point checks output from one INFORMATION INPUT switch (fig. 22, sheet 1 of 3).
2*a*	Operate INFORMATION INPUT P0–P15 switches S2–S17 to the down position.	Same as step 2.	Same as step 2.	True	Steps 2 and 2*a* check both states of all INFORMATION INPUT switches.
3	Operate INFORMATION INPUT P0, P02, P04, P06, P08, P10, P12, and P14 switches S2, S4, S6, S8, S10, S12, S14, and S16 to the up position.	TP6, slot J21C	int	Eight 6.6 microsecond pulses evenly spaced over a 100 microsecond horizontal sweep.	True pulses appear at P01, P03, P05, P07, P09, P11, P13, and P15 digit positions.
3*a*	Operate even numbered INFORMATION INPUT switches to the down position and odd numbered switches to the up position.	Same as step 3	Same as step 3	Same as step 3	True pulses appear at P0, P02, P04, P06, P08, P10, P12, and P14 digit positions. Steps 3 and 3*a* check output of F/F11. If indication is abnormal, proceed to step 4.
4	Same as step 3*a*	TP2, slot J21C	int	Same as step 3*a*	Checks K input to F/F11. If indication is abnormal, check matrix card at slot J20C.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
5	Operate INFORMATION INPUT P0–P15 switches S2–S17 to the down position.	TP5C	int or use multimeter AN/URM–105.	False	Checks output S1–02 of ENTER INFO switch S1 and diode CR2.
5*a*	Press ENTER INFO switch S1 momentarily.	TP6C	Same as step 5	False	Checks output S1–01 of ENTER INFO switch S1 and diode CR1.
6	Operate SLOT SEL LSD switch S18 to position 1. Operate INFORMATION INPUT P0, P02, P04, P06, P08, P10, P12, and P14 switches S2, S4, S6, S8, S10, S12, S14, and S16, to the up position. Press ENTER INFO switch S1.	TB5, slot J13C	+ext Q10 at TB5, slot J16C, 501056 unit.	Eight approximately 6.6 microsecond pulses evenly spaced over a 100 microsecond horizontal sweep.	True pulses appear at P0, P02, P04, P06, P08, P10, P12, and P14 digit positions. Checks output of F/F33. If indication is abnormal, proceed to step 7.
7	Observe indication while ENTER INFO switch S1 is pressed and also while S1 is released.	TP2, slot J13C	+ext Q10 at TB5, slot J16C, 501056 unit.	Complement of indication in step 6 while switch S1 is pressed and released.	Checks input to F/F33 if indication is normal while switch S1 is operated. If indication is abnormal when S1 is operated, check logic at input matrix slot J15C. If indica- is abnormal when switch is released, proceed to step 8.
8	Same as step 7	TP1C	Same as step 7	Same as step 7	Checks recirculation logic from storage function, TM 11–5840–271–30/3.

55. Data Display Control Circuit Troubleshooting

(fig. 7 and 22)

The following chart provides a troubleshooting procedure for the data display control circuit. Steps 2 through 5 check the data control circuit with INFO SELECTOR switch S20 at the TEST position, and steps 6 through 15 check F/F13 logic terms with S20 in the PATCH position. Prior to performing steps 6 through 15, certain test information must be loaded on the test band to provide major cycle coincidence during the test sector. The required test information is loaded on the test band by performing steps 8 and 9 of the operational test procedure in section II. Once the test information is entered on the test band, it will remain unchanged until new information is entered in the same word slots. Test points referenced in this procedure are located on the 501051 unit unless other specified.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
1	Perform initial switch operations (par. 49).	TP15B	−ext P15 at TP30B	6.6 microsecond pulse	Checks presence of P0 for display control gating.
2	Operate SLOT SEL LSD switch S18 to position 1.	TP1B and TP2B	+ext P0 at TP15B	True for 100 microseconds of 3.3 millisecond sweep at both test points.	Checks output of gate amplifiers slot J9C. If indication is normal, proceed to step 6 and if indication is abnormal, proceed to step 2*a*.
2*a*	Same as step 2	TP13B and TP14B	Same as step 2	Same as step 2	Checks input to gate amplifiers slot J9C. If indication is abnormal, proceed to step 3.
3	Same as step 2	TP8, slot J14C	Same as step 2	Same as step 2	Checks input to matrix card slot J11C. If indication is abnormal, proceed to step 4.
4	Same as step 2	TP4, slot J14C	−ext P15 at TP30B	Same as step 2	Checks input to F/F13, slot J14C. If indication is abnormal, proceed to step 5.
5	Same as step 2	TP23C	int or use multimeter AN/URM-105.	True	Checks TEST position of INFO SELECTOR switch S20. If indication is normal, check test band slot selection circuit (par. 53).

Note. Steps 2 through 5 check data control circuit with switch S20 in the TEST position. The remaining steps check F/F13 logic terms with switch S20 in the PATCH position.

6	Perform steps 8 and 9 of operational test, section II. Operate SLOT SEL LSD switch S18 to position 0. Operate INFO SELECTOR switch S20 to the PATCH position.	TP22B	int or use multimeter AN/URM-105.	True	Checks PATCH position of INFO SELECTOR switch S20.
7	Operate ONCE ONLY-EVERY DREV switch S24 to the ONCE ONLY position and return to the EVERY DREV position.	TP24C	Same as step 6	False at ONCE ONLY position, true at EVERY DREV position.	Checks switch S24.
8	None	TP34C, 501056 unit	—ext W07 at TP38C, 501056 unit.	True for 100 microseconds of 10 millisecond horizontal sweep.	Checks presence of test sector OT signal, for data control logic, using test sector OWE signal for synchronization. If indication is abnormal, check DT consoles data entry function (TM 11-5840-271-30/15).
9	Operate ONCE ONLY-EVERY DREV switch S24 to ONCE ONLY position. Operate MAJOR CYCLE SEL UNITS switch S32 to position 8 and MAJOR CYCLE SEL TENS switch S32 to position 6. Press START COMPUTATION switch S26.	TP6, slot J14C	int or use multimeter UN/URM-105.	Goes true when S26 is operated and then goes false in approximately three seconds.	Checks operation of F/F32. If indication is normal, proceed to step 10, and if indication is abnormal, proceed to step 9*a*.
9*a*	Press START COMPUTATION switch S26.	TP2, slot J14C	int	True for less than four milliseconds after S26 is pressed.	Checks K input to F/F32. If indication is abnormal, check data entry circuit (par. 56).

Step	Procedure	Test point	Sync source	Normal indication	Remarks
9*b*	Operate ONCE ONLY-EVERY DREV switch S24 to the EVERY DREV position.	TP1, slot J14C	−ext W07 at TP38C, 501056 unit.	True for 100 microseconds of 10 millisecond horizontal sweep.	Checks one term of F/F32 J input logic. If indication is abnormal, check matrix card slot J15C.
9*c*	Operate ONCE-EVERY DREV switch S24 to the ONCE ONLY position. Press START COMPUTATION switch S26.	TP1, slot J14C	int	Goes true for one word time approximately three seconds after S26 is pressed.	Checks major cycle coincidence term of F/F32 J input logic. If indication is abnormal, proceed to step 10.
10	Operate MAJOR CYCLE SEL UNITS switch S32 and MAJOR CYCLE SEL TENS switch S33 to the 0 positions (fig. 8).	TP8, slot J2C, 501056 unit.	int or use multimeter AN/URM–105.	Goes true and remains true.	Checks output of F/F30.
10*a*	Operate MAJOR CYCLE SEL UNITS switch S32 to position 8 and MAJOR CYCLE SEL TENS switch S33 to position 6. Press START COMPUTATION switch S26.	TP8, slot J2C, 501056 unit.	int	Goes false for 100 microseconds every 10 milliseconds for three seconds, then remains true for approximately 10 milliseconds. Action repeats each time S26 is pressed.	Checks operation of F/F30. If indication is abnormal, proceed to step 11.
11	Same as step 10*a*	TP3, slot J2C, 501056 unit.	int	Goes true for 100 microseconds approximately three seconds after S26 is pressed.	Checks K input to F/F30. If indication is abnormal, proceed to step 12.
12	Operate MAJOR CYCLE SEL TENS switch S33 to 0 position. Operate MAJOR CYCLE SEL UNITS switch S32 to 0 position and then successively to positions 1–9.	TP32C, 501056 unit.	−ext P15 at TP-30B and P0–P08 at TP15B–TP23B successively.	6.6 microsecond pulse	S32 selects P times P0–P09, and is checked by synchronizing each switch position with the previously occurring P time.

13	Operate MAJOR CYCLE SEL UNITS switch S32 to 0 position. Operate MAJOR CYCLE SEL TENS switch S33 successively to positions 0–6 and return to 0 position.	TP33C, 501056 unit.	−ext P15 at TP30B and P0–P05 at TP15B–TP20B successively.	6.6 microsecond pulse	S33 selects P times P0–P06, and is checked by synchronizing each switch position with the previously occurring P time.
14	None	TP36C, 501056 unit.	−ext P01 at TP16B.	100 microsecond false pulses. Recurrence may vary according to number of active tracks at major cycle 1.	Checks presence of major cycle units count signal $\bar{W}05$. If indication is abnormal, check storage function (TM 11–5840–271–30/3).
15	None	TP37C, 501056 unit.	−ext P01 at TP16B.	100 microseconds false pulses. Recurrence may vary according to number of active tracks at major cycle 10.	Checks presence of major cycle tens count signal $\bar{W}06$. If indication is abnormal, check storage function.

56. Display Data Entry Circuit Troubleshooting

The following chart provides a troubleshooting procedure for the display data entry circuits. Steps 1 through 7 check the data entry circuit and steps 8 through 12 check the start computation circuits. Prior to performing steps 1 through 7, a test information word must be entered into test band slot No. 1. The test information word is entered by operating SLOT SEL MSD switch S19 to the 0 position, SLOT SEL LSD switch S18 to position 1, and positioning INFORMATION INPUT P0, P03, P06, P09, P12, and P15 switches S2, S5, S11, S14, and S17 to the up position. All other INFORMATION INPUT switches remain in the down position. Press ENTER INFO switch S1. Test points referenced in this procedure are located on the 501051 unit unless otherwise specified.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
1	Perform initial switch operations (par. 49).	TP1C	+ext Q10 at TB5, slot J16C, 501056 unit.	Complement of 16 bit binary word entered in test band slot No. 1. (0110110110110110).	Checks presence of manual entry band signal W01. If indication is abnormal, check information entry circuit (par. 56).
2	Same as step 1	TP35C	Same as step 1	Sixteen bit binary word entered in test band slot No. 1. (1001001001001001).	Checks output of gate amplifier slot J12C. If indication is normal, proceed to step 3, and if indication is abnormal, proceed to step 2*a*.
2*a*	Same as step 1	TP11B	Same as step 1	Same as step 2	Checks input to gate amplifier slot J12C. If indication is abnormal, proceed to step 2*b*.
2*b*	Same as step 1	TP8, slot J21C	Same as step 1	Same as step 2	Checks Q output of F/F12 slot J21C. If indication is abnormal, proceed to step 4.
3	Same as step 1	TP38C	Same as step 1	Complement of 16 bit binary word entered in test band slot No. 1.	Checks output of gate amplifier slot J10C. If indication is normal, proceed to step 4, and if indication is abnormal, proceed to step 3*a*.
3*a*	Same as step 1	TP12B	Same as step 1	Same as step 3	Checks input to gate amplifier slot J10C. If indication is abnormal, proceed to step 3*b*.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
3*b*	Same as step 1	TP7, slot J21C	Same as step 1	Same as step 3	Checks $\bar{Q}$ output of F/F12 slot J21C. If indication is abnormal, proceed to step 4.
4	Same as step 1	TP3, slot J21C	Same as step 1	Same as step 3	Checks K input to F/F12 slot J21C. If indication is abnormal, proceed to step 5.
5	Same as step 1	TP23C	int or use multimeter AN/URM–105.	True	Checks INFO SELECTOR switch S32 output at TEST position.
6	Operate INFO SELECTOR switch S20 to PATCH position.	TP22C	int or use multimeter AN/URM–105.	True	Checks INFO SELECTOR switch S20 output at PATCH position.
7	Connect patch board test probe S25 to P01 time at TP16B. *Note.* Steps 1 through 7 check data entry circuit and the remaining steps check the start computation circuit.	TP25C	−ext P0 at TP15B.	6.6 microsecond pulse	Checks patch board test probe S25. If indication in steps 5, 6, and 7 are normal, check matrix card slot J20C.
8	Initial switch operations (par. 49).	TP29B	−ext P13 at TB28P.	6.6 microsecond pulse	Checks presence of P14 time for start computation timing.
9	No procedure required	TP2C	−ext TP38C 501056 unit.	100 microsecond pulse	Checks presence of test sector OT signal W03 for start computation timing. If indication is abnormal, check DT consoles data entry function (TM 11–5840–271–30/15).
10	Press START COMPUTATION switch S26.	TP8, slot J16C	int	True for less than 4 milliseconds after S26 is pressed.	Checks output of F/F31, slot J16C.

11	Same as step 10	TP26C	int or use multimeter AN/URM 105.	False while S26 is pressed and true while S26 is not pressed.	Checks START COMPUTATION switch S26 and the J′ input to F/F31.
12	Operate SLOT SEL LSD switch S18 to position 7. Operate SLOT SEL MSD switch S19 to position 3. Press START COMPUTATION switch S26.	TP3, slot J16C	+ext Q10 at TP5, slot J16C, 501056 unit.	6.6 microsecond true pulse after S26 is operated.	Checks K input to F/F31. If indication is abnormal, check test band slot selection circuit (par. 53) and matrix card slot J15C.

57. Display Register Circuit Troubleshooting

(fig. 10 and 22)

The following chart provides a troubleshooting procedure for the display register circuit. Prior to performing this procedure, a test information word must be entered into test band slot No. 1. The test information word is entered by operating SLOT SEL MSD switch S19 to the 0 position, SLOT SEL LSD switch S18 to position 1, and positioning INFORMATION INPUT P0, P03, P06, P09, P12, and P15 switches S2, S5, S8, S11, S14, and S17 to the up position. All other INFORMATION INPUT switches remain in the down position. Press ENTER INFO switch S1. Test points referenced in this procedure are located on the 501056 unit unless otherwise specified.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
1	Perform initial switch operations (par. 49).	TP15B through TP30B successively.	−ext P15 at TP30B and at P0 through P14 at TP15B through TP29B successively.	6.6 microseconds	Checks presence of P times P0 through P15 when each P time is synchronized with the previously occurring P time.
2	Operate SLOT SEL LSD switch S18 to position 1.	TP19C and TP20C	+ext P01 at TP16B, 501051 unit.	True for 100 microseconds of a 3.3 millisecond sweep at each test point.	Checks presence of data control signals G1Q13 and G2Q13 at display register. If indication is abnormal, check data control circuit (par. 55).
3	Same as step 2	TP17C	+ext Q10 at TP5B, slot J16C.	Sixteen bit binary word entered in test band slot No. 1 (1001001001001001).	Checks presence of data entry signal GQ12 at display register. If indication is abnormal, check data entry circuit (par. 56).
4	Same as step 2	TP18C	Same as step 3	Complement of 16 bit binary word entered in test band slot No. 1. (0110110110110110).	Checks presence of data entry signal G$\bar{Q}$12 at display register. If indication is abnormal, check data entry circuit (par. 56.)
5	Operate INFORMATION INPUT P0 through P15 switches S2 through S17 to the up position. Press ENTER INFO switch S1.	TP1C through TP16C successively.	int or use multimeter AN/URM–105.	False at each test point	Test points TP1C through TP16C check display indicators P0 through P15 respectively.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
6	Operate INFORMATION INPUT P0 through P15 switches S2 through S17 to the down position. Press ENTER INFO switch S1.	Same as step 5	Same as step 5	True at each test point	Test points TP1C through TP3C check output of gate amplifier, slot J7C and matrix card slot J6C. Test points TP9C through TP16C check output of gate amplifier at slot J8C and matrix card at slot J6C.
7	Same as step 6	TP7, slot J16C; TP6, slot J14C, TP7, slot J14C; TP6, slot J13C; TP7, slot J13C; TP6, slot J12C; TP7, slot J12C; and TP6, slot J10C, successively.	Same as step 5	True at each test point	Checks true state output of F/F14 through F/F21, input to matrix card at slot J6C, and gate amplifier at slot J7C.
8	Same as step 5	Same as step 7	Same as step 5	False at each test point	Checks false state output of F/F14 through F/F21, input to matrix card at slot J6C, and gate amplifier at slot J7C.
9	Same as step 5	TP7, slot J10C; TP6, slot J9C; TP7, slot J9C; TP6, slot J5C; TP7, slot J5C; TP6, slot J3C; TP7, slot J3C; and TP6, slot J2C successively.	Same as step 5	False at each test point	Checks false state output of F/F22 through F/F29, input to matrix card at slot J6C, and gate amplifier at slot J8C.
10	Same as step 6	Same as step 9	Same as step 5	True at each test point	Checks true state output of F/F32 through

					F/F29, input to matrix card at slot J6C, and gate amplifier at slot J8C.
11	Same as step 6	TP3, slot J16C; TP2, slot J14C; TP3, slot J14C; TP2, slot J13C; and TP3, slot J13C successively.	−ext P0 at TP15B, P01 at TP16B, P02 at TP17B, P03 at TP18B, and P04 at TP19B on 501051 unit successively.	6.6 microsecond true pulses.	Checks K input to F/F14 through F/F18 when each input is synchronized with previously occurring P time. If indication is abnormal, check matrix card at slot J15C.
12	Same as step 6	TP2, slot J12C; TP3, slot J12C; TP2, slot J10C; TP3, slot J10C; TP2, slot J9C; and TP3, slot J9C successively.	−ext P05 at TP20B, P06 at TP21B, P07 at TP22B, P08 at TP23B, P09 at TP24B, and P10 at TP25B on 501051 unit successively.	6.6 microsecond true pulses.	Checks K input to F/F19 through F/F24 when each input is synchronized with previously occurring P time. If indication is abnormal, check matrix card at slot J11C.
13	Same as step 6	TP2, slot J5C; TP3, slot J5C; TP2, slot J3C; TP3, slot J3C; and TP2, slot J2C successively.	−ext P11 at TP26B, P12 at TP27B, P13 at TP28B, P14 at TP29B, and P15 at TP30B.	6.6 microsecond true pulses.	Checks K input to F/F25 through F/F29 when each input is synchronized with previously occurring P time. If indication is abnormal, check matrix card at slot J4C.
14	Same as step 5	TP4, slot J16C; TP1, slot J14C; TP4, slot J14C TP1, slot J13C; and TP4, slot J13C successively.	Same as step 11	6.6 microsecond true pulses.	Checks J input to F/F14 through F/F18 when each input is synchronized with previously occurring P time. If indication is abnormal, check matrix card at slot J15C.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
15	Same as step 5	TP1, slot J12C; TP4, slot J12C; TP1, slot J10C; TP4, slot J10C; TP1, slot J9C; and TP4, slot J9C successively.	Same as step 12	6.6 microsecond true pulses.	Checks J input to F/F19 through F/F24 when each input is synchronized with previously occurring P time. If indication is abnormal, check matrix card at slot J11C.
16	Same as step 5	TP1, slot J5C; TP4, slot J5C; TP1, slot J3C; TP4, slot J3C; and TP1, slot J2C successively.	Same as step 13	6.6 microsecond true pulses.	Checks J input to F/F25 through F/F29 when each input is synchronized with previously occurring P time. If indication is abnormal, check matrix card at slot J4C.

58. Reject ARDME Circuit Troubleshooting

The following chart provides a troubleshooting procedure for the reject ARDME data circuit.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
1	Momentarily connect jumper wire between test point TP34C on 501056 unit and test point TP8A on 501051 unit. Repeat this procedure several times if necessary.	TP23B, 501056 unit	int or use multimeter AN/URM-105.	+28 volts for 2 seconds after momentarily connecting jumper wire.	Checks REJECT ARDME DATA indicator lamp DS17. If indication is abnormal, check ARDME malfunction pulse stretcher, slots J19C through J21C of 501056 unit.

CHAPTER 6
DIGITAL DATA DISPLAY FUNCTION TROUBLESHOOTING

Section I. PRELIMINARY PROCEDURE

59. General

This section contains the procedure for equipment setup and initial switch operations for the digital data display function. This procedure is accomplished before performing the operational test contained in section II. The circuit troubleshooting procedures contained in section III also use this procedure. This procedure establishes a state of the equipment prior to test, and prevents unnecessary repetition of switch settings and abnormal indications because of incorrect switch settings. Instructions in paragraph 3 of this section are referred to during test procedures in order to return all switches to a neutral or common starting position.

60. Equipment Setup

a. Pull out unit drawer 501051 to provide access to the digital data display function control panel, level B. Pull out unit drawer 501056 to provide access to the TCC STEP SELECTOR switches, level B, and the flip-flop card assembly test points.

b. Set up oscilloscope AN/USM-81 as per TM 11-6625-219-12.

c. Check that power is supplied to the digital data function.

61. Initial Switch Operations

The following chart lists the digital data display function switches and the operation which positions each switch at a neutral or common starting position. All switches listed in the following chart are located on the digital data display function control panel at level B of the 501051 unit, with the exception of the program step selector switches. The program step selection switches are MAJOR TENS switch S2, MAJOR UNITS switch S1, and MINOR switch S3. These three switches are located on the 501056 unit at level B.

Step	Switch name	Switch No.	Operation
1	SN SELECT	S04 through S10	Operate to down position.
2	DISPLAY GATE TIMING	S02	Operate CCW to SN position.
3	CONTINUOUS HOLD	S11	Operate to CONTINUOUS position.
4	MAJOR UNITS	S1	Operate fully CCW.
5	MAJOR TENS	S2	Operate fully CCW.
6	MINOR	S3	Operate fully CCW.
7	START DISPLAY	S01	Listed for reference purposes only.
8	SPECIAL GATE/A1-A8	S03-01 through S03-08	Listed for reference purposes only.

Section II. OPERATIONAL TEST

62. General

This section contains a complete operational test procedure which is used to determine whether a malfunction exists in the digital data display function circuits. Each step of the test procedure is performed sequentially unless an abnormal indication is obtained. The repairman can isolate an indicated malfunction by using the circuit troubleshooting procedure referenced in the remarks column of the operational test. After repair action is taken, the operational test is repeated from the beginning to determine whether any further malfunctions exist.

63. Operational Test Procedure

(fig. 16)

a. The following chart provides a procedure for entering known test information on the storage function test band. This information is used during the operational test of the digital data display function. Switches and indicator lamps listed in the following chart are located on, and are part of, the tracking computer test function control panel (ch 5, sec I). The tracking computer test function switches are not used during any other portion of this test procedure.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
1	Operate INFO SELECTOR switch S20 to the TEST position. Operate SLOT SEL LSD switch S18 to position 1 and SLOT SEL MSD switch S19 to position 0. Operate INFORMATION INPUT P0, P01, P04, P05, P08, P09, P12, and P13 switches S2, S3, S6, S7, S10, S11, S14, and S15 to the up position. Press ENTER INFO switch S1.	None	None	DISPLAY REGISTER indicators P0, P01, P04, P05, P08, P09, P12, and P13 glow and indicators P02, P03, P06, P07, P10, P11, P14, and P15 do not glow.	Indicates information word 0011001100110011 is entered on test band.
2	Operate SLOT SEL LSD switch S18 and SLOT SEL MSD S19 successively to each of the remaining 36 octal positions. Press ENTER INFO switch S1 at each selected position of the SLOT SEL switches.	None	None	Same as step 1 each time S1 is pressed.	Steps 1 and 2 enter the same known test information word into every slot of the test band (manual entry band). The manual entry band is used during the remainder of the digital data display function operational test to provide known input information.

b. The following chart lists the complete operational test procedure for the digital data display function. Chapter 4 must be read prior to performing this test procedure. Oscilloscope AN/USM-81 is used extensively throughout this test and is connected as listed in the test point and sync source columns. The test points listed in both columns are located on the 501056 unit unless otherwise specified. Paragraph numbers appearing in the remarks column refer to the circuit troubleshooting procedure used to isolate a malfunction. Read all instructions pertaining to each step before connecting the oscilloscope or performing the listed procedures. All pulse width and repetition rate indications are listed as approximate values.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
1	Perform initial switch operations (par. 61). Insert patch board test probe S12 into test jack J57.	TP3A and TP4A	int	True for 13 microseconds and false for 13 microseconds continuously at both test points.	Checks display register data input circuit. If indication is abnormal, see paragraph 65.
2	Disconnect patch board test probe S12. Operate SN SELECT LSD switch S04, 3d LSD switch S06, 5th LSD switch S08, and MSD switch S10 to the up position (LSD switch is at the right and MSD switch is at the left.)	TP2A and then TP1A.	−ext P08 at TP15B.	Seven bit word (1010101) at TP2A recurring every 55 microseconds. Complement of seven bit word (0101010) at TP1A recurring every 55 microseconds.	Checks sector number selection circuit. If indication is abnormal, see paragraph 66. *Note.* SN SELECT switches remain at selected position during completion of test.
3	Same as step 2	TP7, slot J20A	−ext P15 at TB22P.	True during P0 every 10 milliseconds.	Checks input data timing for sector number selection circuit. If indication is abnormal, see paragraph 66.
4	Operate DISPLAY GATE TIMING switch S02 to SPECIAL position. Connect a jumper wire between P08 test point TP15B and SPECIAL GATE TEST jacks JA1 through JA8 successively.	TP7, slot J20A	int	True for 50 microseconds and false for 50 microseconds continuously with P08 routed to each SPECIAL GATE test jack.	Checks special gate timing circuit. If indication is abnormal, see paragraph 67. *Note.* Jumper wire remains connected to any test jack during completion of test.
5	Operate DISPLAY GATE TIMING switch S02 to SN position.	TP7, slot J20A	−ext P15 at P22B	True during P0 only when the selected major and minor cycle occur during the selected sector.	Checks program step selection circuit. If indication is abnormal, see paragraph 68.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
	Operate MAJOR TENS switch S2 to position 2. Operate MAJOR UNITS switch S1 to position 2. Operate MINOR switch S3 to position 2.			Must recur at least once every 6 seconds.	
6	Operate MAJOR TENS switch S2, MAJOR UNITS switch S1, and MINOR switch S3 fully CCW. Press START DISPLAY switch S01.	TP8, slot J18A	int	True for 100 microseconds every 10 milliseconds.	Partially checks display register control circuit. If indication is abnormal, see paragraph 69.
7	Operate DISPLAY GATE TIMING switch to the SPECIAL position. Press START DISPLAY switch S01.	Same as step 6	Same as step 6	True for 100 microseconds each time S01 is pressed.	Partially checks display register control circuit. If indication is abnormal, see paragraph 69.
8	Insert patch board test probe S12 into test jack J57.	None	None	DISPLAY REGISTER indicators P0, P01, P04, P05, P08, P09, P12, and P13 glow and indicators P02, P03, P06, P07, P10, P11, P14, and P15, do not glow.	Partially checks display register circuit. If indication is abnormal, see paragraph 70.
9	Insert patch board test probe S12 into test point TP10A on 501051 unit. Press START DISPLAY switch S01.	None	None	All DISPLAY REGISTER indicators glow.	Partially checks display register circuit. If indication is abnormal, see paragraph 70.
10	Insert patch board test probe S12 into test	None	None	All DISPLAY REGISTER indi-	Partially checks display register circuit. If

	point TP8A on 501051 unit. Press START DISPLAY switch.			cator lamps extinguish.	indication is abnormal, see paragraph 70.
11	Disconnect patch board test probe S12.	TP2B and TP3B	int	152 kc clock pulse at each test point.	Checks output from clock pulse regenerator at slot J11B and J6B respectively. If indication is abnormal, proceed to step 11*a*.
11*a*	None	TP1B	int	152 kc clock pulse	Checks input into clock pulse regenerators. If indication is abnormal, check timing function (TM 11–5840–271–30/3).

Section III. DIGITAL DATA DISPLAY FUNCTION CIRCUIT TROUBLESHOOTING

64. General

This section contains circuit troubleshooting procedures which aid the repairman to isolate the malfunctions of the digital data display function circuits to a card assembly or subassembly. Each circuit troubleshooting procedure is presented in a separate paragraph. The paragraphs are each referenced from the operational test in section II, so it is assumed in all procedures that a malfunction is known to exist. The oscilloscope is used extensively in all circuit troubleshooting procedures, and is connected as indicated in the test point and sync source columns. A multimeter may be used for steady state indications as indicated in the sync source column. All pulse width and repetition rate indications are listed as approximate values. Read all instructions pertaining to each step before performing operations listed in the procedure column. Perform all step procedures sequentially unless instructions in the remarks column specify otherwise.

65. Display Register Data Input Circuit Troubleshooting

(fig. 15 and 23)

The following chart provides the circuit troubleshooting procedure for the display register data input circuit. Test points referenced in this procedure are located on the 501056 unit.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
1	Perform initial switch operations (par. 61). Connect patch board test probe to P01 time test point TP8B on 501056 unit.	TP3A	int	6.6 microsecond pulse recurs every 100 microseconds.	Checks GQ07 output from gate amplifier, slot J3A. If indication is normal, proceed to step 2.
2	Same as step 1	TP5, slot J6A	int	Same as step 1	Checks Q07 input to gate amplifier, slot J3A through matrix card, slot J4A. If indication is abnormal, proceed to step 5.
3	Same as step 1	TP4A	int	Complement of step 1 indication.	Checks G$\bar{Q}$07 output from gate amplifier, slot J3A. If indication is abnormal, proceed to step 4.
4	Same as step 1	TP6, slot J6A	int	Same as step 3	Checks $\bar{Q}$07 input to gate amplifier, slot J3A through matrix card, slot J4A. If indication is abnormal, proceed to step 5.
5	Same as step 1	TP2, slot J6A	int	Same as step 3	Checks input to F/F07, slot J6A. If indication is abnormal, proceed to step 6.
6	Same as step 1	TP32A	int	Same as step 3	Checks S12–01 input to matrix card, slot J4A. If indication is abnormal, proceed to step 7.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
7	Disconnect test probe from test point TP8B.	TP8B	int	Same as step 3	Checks presence of P time P01. If indication is normal, check between test point TP32A and test probe for continuity.

66. Sector Number Selection Circuit Troubleshooting

(fig. 16, 17, and 23)

The following chart provides the circuit troubleshooting procedure for the sector number selection circuit. Steps 1 through 11 check the sector number selection circuit and steps 12 through 16 check the input data timing using sector selection. Test points referenced in this procedure are located on the 501056 unit.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
1	Perform initial switch operation (par. 61).	TP16B, TP17B, TP18B, TP19B, TP20B, TP21B, and TP22B successively.	−ext TP15B, TP16B, TP17B, TP18B, TP19B, TP20B, and TP21B successively.	6.6 microsecond pulse	Checks presence of P times P09 through P15 for sector number selection when each P time is synchronized with the previously occurring P time.
2	Operate the seven SN SELECT switches, S04 through S10, to the up position.	TP2A	int	Seven consecutive 6.6 microsecond true pulses recurring every 55 microseconds.	Checks G02 output of gate amplifier, slot J3C. If indication is normal proceed to step 4, and if indication is abnormal proceed to step 3.
3	Same as step 2	TP18A, TP20A, TP22A, TP24A, TP26A, TP28A, and TP 30A successively.	int or use multimeter AN/USM–105.	True indication at each test point.	Checks −02 output signal from S04 through S10 when indication is abnormal, and checks input to gate amplifier, slot J3A through matrix card, slot J4A when indications are all normal.
4	Same as step 2	TP1A	int	Seven consecutive 6.6 microsecond false pulses recurring every 55 microseconds.	Checks G01 output of gate amplifier, slot J3C. If indication is normal proceed to step 6, and if indication is abnormal, proceed to step 5.
5	Same as step 2	TP17A, TP19A, TP21A, TP23A, TP25A, TP27A, and TP29A successively.	int or use multimeter AN/URM–105.	False indication at each test point.	Checks −01 output signal from S04 through S10 when indication is abnormal, and checks input to gate amplifier, slot J3A through matrix card, slot J4A

					when indications are all normal.
6	Operate the seven SN SELECT switches S04 through S10 to the down position.	TP2A	int	Same as step 4	Checks G02 output of gate amplifier, slot J3C. If indication is normal proceed to step 8, and if indication is abnormal proceed to step 7.
7	Same as step 6	TP18A, TP20A, TP22A, TP24A, TP26A, TP28A, and TP30A successively.	int or use multimeter AN/URM–105.	False indication at each test point.	Checks –02 output signal from S04 through S10 when indication is abnormal, and checks input to gate amplifier, slot J3A through matrix card, slot J4A when indications are all normal.
8	Same as step 6	TP1A	int	Same as step 2	Checks G01 output of gate amplifiers, slot J3C. If indication is normal proceed to step 10, and if indication is abnormal proceed to step 9.
9	Same as step 6	TP17A, TP19A, TP21A, TP23A, TP25A, TP27A and TP29A successively.	int or use multimeter AN/USM–105.	True indication at each test point.	Checks output signal from S04 through S10 when indication is abnormal, and checks input to gate amplifier, slot J3A through matrix card, slot J4A when indications are all normal.
10	Operate DISPLAY GATE TIMING switch S02 to the SPECIAL position and return to the SN position.	TP7A	Same as step 9	Indication is false when S02 is at the SPECIAL position and true when S02 is at the SN position.	Checks S02–01 output signal from S02. S02 remains in the SN position through the completion of test.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
11	Operate SN SELECT LSD switch S04, 3rd LSD switch S06, 5th LSD switch S08, and MSD switch S10 to the up position. Every other switch remains in the down position.	TP33A	+ext G02 at TP2A	Seven bit binary word 1010101. Word recurs every 10 milliseconds.	Partially checks selected sector number coincidence with sector number OWE signal W01. If indication is abnormal, check timing function (TM 11-5840-271-30/3).
11*a*	Same as step 11	TP34A	+ext G01 at TP1A	Complement of indication in step 11: 0101010.	Partially checks selected sector number coincidence with sector number OWE signal W01. If indication is abnormal, check timing function (TM 11-5840-271-30/3).
11*b*	Operate SN SELECT 2nd LSD switch S05, 4th LSD switch S07, and 6th LSD switch S09 to the up position, and operate the four remaining switches to the down position.	TP33A	+ext G02 at TP2A	Complement of indication in step 11: 0101010.	Partially checks selected sector number coincidence with sector number OWE signal W01. If indication is abnormal, check timing function (TM 11-5840-271-30/3).
11*c*	Same as step 11*b*	TP34A	+ext G01 at TP1A	Same as step 11	Partially checks selected sector number coincidence with sector number OWE signal W01. If indication is abnormal, check timing function (TM 11-5840-271-30/3).
12	Operate SN SELECT switches S04 through S10 to the down position.	TP7B	+ext P15 at TP22B	6.6 microsecond pulse	Checks presence of P0 for input data timing.

13	Operate SN SELECT LSD switch S04 to the up position. All other SN SELECT switches remain down.	TP7, slot J20A	+ext P09 at TP16B	True for 100 microseconds every 10 milliseconds.	Checks Q output from F/F06, slot J20A. If indication is normal proceed to step 14, and if indication is abnormal proceed to step 15.
14	Same as step 13	TP8, slot J20A	Same as step 13	False for 100 microseconds every 10 milliseconds.	Checks $\bar{Q}$ output from F/F06, slot J20A. If indication is abnormal, proceed to step 15.
15	Operate SN SELECT LSD switch S04 to the down position. All SN SELECT switches remain in the down position.	TP3, slot J20A	−ext P08 at TP15B	6.6 microsecond true pulse recurring every 200 microseconds of a 10 millisecond sweep.	Checks K input to F/F06, slot J20A. If indication is abnormal, check matrix card, slot J19A.
16	Same as step 15	TP4, slot J20A	−ext P15 at TP22B	6.6 microsecond true pulse recurring every 100 microseconds.	Checks J input to F/F06, slot J20A. If $\bar{Q}$06 goes true and J06 is abnormal, check matrix card, slot J19A.

67. Special Gate Timing Circuit Troubleshooting

(fig. 16 and 23)

The following chart provides the circuit troubleshooting procedure for the special gate timing circuit. Test points referenced in this procedure are located on the 501056 unit.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
1	Perform initial switch operations (par. 61).	TP7B	—ext P15 at TP22B	6.6 microsecond pulses	Checks presence of P0 for input data timing.
2	Operate DISPLAY GATE TIMING switch S02 from the SN position to the SPECIAL position.	TP8A	int or use multimeter AN/URM–105.	Indication is false when S02 is at the SN position and true when S02 is at the SPECIAL position.	Checks S02–02 output signal from S02. S02 remains at the SPECIAL position through the completion of test.
3	None	TP7 and TP8, slot J20A.	int or use multimeter AN/URM–105.	False at TP7 and true at TP8.	Partially checks Q and $\bar{Q}$ outputs from F/F06, slot J20A. If indication is abnormal, proceed to step 4.
3*a*	Connect a jumper wire between P08 test point TP15B and SPECIAL GATE test jack JA1.	Same as step 3	int	True for 50 microseconds and false for 50 microseconds continuously at both test points.	Partially checks Q and $\bar{Q}$ outputs from F/F06, slot J20A. If indication is abnormal, proceed to step 4.
4	Connect a jumper wire between P08 test point TP15B and successively to each of the following SPECIAL GATE test jacks: JA1, JA2, JA3, JA4, JA5, JA6, JA7, and JA8.	TP4, slot J20A	—ext P07 at TP14B	6.6 microsecond pulses at each test jack.	Checks J input to F/F06, slot J20A and output from matrix card, slot J19A. If indication is abnormal, proceed to step 6.
5	None	TP3, slot J20A	—ext P15 at TP22B	6.6 microsecond pulses	Checks K input to F/F06, slot J20A. If Q06 goes true and K06 is abnormal, check matrix card, slot J19A.
6	Connect a jumper wire between P08 test point TP15B and SPECIAL GATE test jack JA1. Connect jumper wire between SPECIAL	TP9A through TP16A.	Same as step 4	6.6 microsecond pulses at each of the eight test points.	Checks matrix card, slot J19A. If any indication is abnormal, check continuity between associated test point and test jack.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
	GATE test jacks JA1 through JA8 so that all test jacks receive the P08 signal.				

68. Program Step Selection Circuit Troubleshooting

(fig. 16, 18, and 23)

The following chart provides the circuit troubleshooting procedure for the program step selection circuit. Test points referenced in this procedure are located on the 501056 unit. MAJOR UNITS, MAJOR TENS, and MINOR switches S1, S2, and S3 respectively are located on level B of the 501056 unit.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
1	Perform initial switch operations (par. 61).	TP8B–TP22B successively.	−ext P0–P14 at TP7B–P21B successively.	6.6 microsecond pulses	Checks presence of P times P01–P15 when each P time is synchronized with the previously occurring P time.
2	None	TP6, slot J21B	−ext P04 at TP11B	6.6 microsecond pulse recurs at least once every six seconds, depending upon the number of active tracks at MC 50.	Checks $\overline{Q}$ output from F/F25, slot J21B. If indication is normal proceed to step 3, and if indication is abnormal proceed to step 4.
3	None	TP5, slot J21B	Same as step 2	6.6 microsecond pulse occurs as complement to step 2 indication.	Checks Q output from F/F25, slot J21B. If indication is normal proceed to step 6, and if indication is abnormal proceed to step 4.
4	None	TP2, slot J21B	Same as step 2	Same as step 2	Checks input to F/F25, slot J21B. If indication is abnormal proceed to step 5.
5	None	TP36C	Same as step 2	Same as step 2	Checks matrix of slot J14B. If indication is abnormal, check storage function (TM 11–5840–271–30/3).
6	None	TP7, slot J21B	Same as step 2	6.6 microsecond pulse recurs at least once every six seconds, depending upon the number of active tracks at MC 5.	Checks output of F/F26, slot J21B. If indication is normal proceed to step 9, and if indication is abnormal proceed to step 7.

7	None	TP3, slot J21B	Same as step 2	Same as step 6	Checks input to F/F26, slot J21B. If indication is abnormal proceed to step 8.
8	None	TP37C	Same as step 2	Same as step 6	Checks matrix of slot J14B. If indication is abnormal, check storage function (TM 11-5840-271-30/3).
9	Operate DISPLAY GATE TIMING switch S02 to the SPECIAL position. Connect a jumper wire between P08 test point TP15B and SPECIAL GATE test jack A1.	TP7, slot J20A	int	True for 50 microseconds and false for 50 microseconds continuously.	Checks operation of F/F06 slot J20A. If indication is abnormal, check special gate timing circuit (par. 67).
10	Disconnect jumper wire from SPECIAL GATE test jack A1 but do not change position of DISPLAY GATE TIMING switch S02. Operate MAJOR TENS switch S2 to position 0–6 successively and return to 0 position.	TP7, slot J20A	+ext P0–P06 at TP7B–TP13B successively.	6.6 microsecond pulse recurs every 100 microseconds except when the selected major cycle occurs.	Checks operation of S2 when switch positions 0–6 are synchronized with P times P0–P06 respectively.
11	Operate MAJOR UNITS switch S1 to positions 0–9 successively and return to 0 position.	TP7, slot J20A	+ext P0–P09 at TP7B–TP16B successively.	6.6 microsecond pulse recurs every 100 microseconds except when the selected major cycle occurs. MC 2 and MC 9 are 13 DREV operations, so the pulse does not recur for 130 milliseconds during major cycle coincidence.	Checks operation of switch S3 when switch positions 1–12 are synchronized with P times P0–P09 respectively.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
12	Operate MAJOR UNITS switch S1 to position 2 (13 DREV operation). Operate MINOR switch S3 to positions 1–12 successively.	TP7, slot 20A	+ext P11 at TP18B.	6.6 microsecond pulse recurs every 200 microseconds of the 13 DREV operation except when the selected minor cycle occurs.	Checks operation of switch S3 when switch positions 1–12 are synchronized with the minor cycle count LSD.

69. Display Register Control Circuit Troubleshooting

(fig. 19 and 23)

The following chart provides the circuit troubleshooting procedure for the display register control circuit. Test points referenced in this procedure are located on the 501056 unit.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
1	Perform initial switch operations (par. 61).	TP7B	−ext P15 at TP22B.	6.6 microsecond pulses	Checks presence of P0 for start display timing.
2	Operate DISPLAY GATE TIMING switch S02 to the SPECIAL position. Connect a jumper wire between P14 test point TP21B and SPECIAL GATE test jack A1.	TP7, slot J20A	−ext P15 at TP23B.	6.6 microsecond pulses	Checks operation of F/F06, slot J20A. If indication is abnormal, check special gate timing circuit (par. 67). *Note.* Step 2 procedures assure a true Q06 signal during P0 for the remainder of test.
3	Operate CONTINUOUS HOLD switch S11 to the HOLD position. Press START DISPLAY switch S01.	TP8, slot J18A	int	Goes true for 100 microseconds each time S01 is operated.	Checks output from F/F08, slot J18A. If indication is normal proceed to step 5, and if indication is abnormal proceed to step 4.
4	Same as step 3	TP4, slot J18A	int	6.6 microsecond pulse each time S01 is pressed.	Checks J input to F/F08, slot J18A. If indication is abnormal, proceed to step 5.
4*a*	Same as step 3	TP3, slot J18A	int	Same as step 4	Checks K input to F/F08, slot J18A. If Q08 goes true and K08 is abnormal, check matrix card slot J19A.
5	Operate CONTINUOUS HOLD switch S11 to CONTINUOUS position. Press START DISPLAY switch S01.	TP5, slot J20A	int or use multimeter AN/URM-105.	Goes true and remains true.	Partially checks output from F/F05, slot J20A. If indication is normal proceed to step 5*b*, and if indication is abnormal proceed to step 5*a*.

5*a*	Press START DISPLAY switch S01.	TP6A	Same as step 5	False while S01 is pressed and true when S01 is not pressed.	Checks S01–01 output from switch S01 if indication is abnormal. If indication is normal, check F/F05 at slot J20A and then the matrix card at slot J19A.
5*b*	Operate CONTINUOUS HOLD switch S11 to the HOLD position.	TP5, slot J20A	Same as step 5	Goes false when S11 is pressed.	Partially checks output from F/F05, slot J20A. If indication is abnormal proceed to step 5*c*.
5*c*	Operate CONTINUOUS HOLD switch S11 to the CONTINUOUS position.	TP31A	Same as step 5	True while S11 is at HOLD position and false while S11 is at CONTINUOUS position.	Checks S11–01 output signal from S11 if indication is abnormal. If indication is normal, check F/F05 at slot J20A and then the matrix card at J19A.

70. Display Register Circuit Troubleshooting

(fig. 20 and 23)

The following chart provides the circuit troubleshooting procedure for the display register circuit. Test points referenced in this procedure are located on the 501056 unit.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
1	Perform initial switch operations (par. 61).	TP7B–RP22B successively.	—ext P15 at TP22B and TP7B–TP21B successively.	6.6 microsecond pulse	Checks presence of P times P0–P15 when each P time is synchronized with the previously occurring P time.
2	Connect patch board test probe S12 to test point TP10A on 501051 unit.	TP3A and TP4A	int or use multimeter AN/URM–105.	True at TP3A and false at TP4A.	Checks presence of GQ07 and GQ̄07 signals for data input to display register. If indication is abnormal, check data input circuit (par. 65).
3	Operate DISPLAY GATE TIMING switch S02 to the SPECIAL position. Connect a jumper wire between P14 test point TP21B and SPECIAL GATE test jack A1. Operate CONTINUOUS HOLD switch S11 to the HOLD position. Press START DISPLAY switch S01.	TP5A	int	Goes true for 100 microseconds each time S01 is operated.	Checks presence of GQ08 signal for display control and output from gate amplifier, slot J3A. If indication is normal proceed to step 5, and if indication is abnormal, proceed to step 4.
4	Same as step 3	TP8, slot J18A	int	Same as step 3	Checks input to gate amplifier at slot J3A through matrix card at slot J4A. If indication is abnormal, check display register control circuit.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
5	Same as steps 2 and 3	None	None	DISPLAY REGISTER indicators 0–15 glow.	Partially checks display register. If indication is normal proceed to step 5*a*, and if indication is abnormal proceed to step 6.
5*a*	Connect patch board test probe S12 to test point TP8A on 501051 unit. Press START DISPLAY switch S01.	None	None	DISPLAY REGISTER indicators 0–15 extinguish.	Partially checks display register. If indication is abnormal proceed to step 6.
6	Same as steps 2 and 3	TP6, slot J18A; TP7, slot J17A; TP6, slot J17A; TP7, slot J16A; TP6, slot J16A; TP7, slot J14A; TP6, slot J14A; TP7, slot J12A; TP6, slot J12A; TP7, slot J11A; TP6, slot J11A; TP7, slot J8A; TP6, slot J8A; TP7, slot J9A; TP6, slot J9A; and TP7, slot J5A successively.	int or use multimeter AN/USM–105.	False (−6 volts) at each test point.	Checks DISPLAY REGISTER indicator lamps 0–15 and output from display flip-flops, F/F09–F/F24, respectively. If any indication is abormal proceed to step 7, and if indications are normal proceed to step 6*a*.
6*a*	Connect patch board test probe S12 to test point TP8A on 501051 unit. Press START DISPLAY switch S01.	Same as step 6	Same as step 6	True (Ov) at each test point.	Checks output from display register flip-flops, F/F09–F/F24, respectively. If indication is abnormal proceed to step 7.
7	Same as steps 2 and 3	TP1, slot J18A; and TP4, slot	int	6.6 microsecond tire pulse each time S01	Checks J input to F/F09 and F/F10 respec-

		J17A.		is pressed.	tively. If indication is abnormal, check matrix card, slot J19A.
8	Same as steps 2 and 3	TP1, slot J17A; TP4, slot J16A; TP1, slot J16A; TP4, slot J14A; TP1, slot J14A; and TP4, slot J12A.	int	Same as step 7	Checks J input to F/F11–F/F16 respectively. If indication is abnormal, check matrix card, slot J15A.
9	Same as steps 2 and 3	TP1, slot J12A; TP4, slot J11A; TP1, slot J11A; TP4, slot J8A; TP1, slot J8A; TP4, slot J9A; TP1, slot J9A; and TP4, slot J5A.	int	Same as step 7	Checks J input to F/F17–F/F24 respectively. If indication at TP1, slot J9A is abnormal, check matrix card at slot J15A; if indication at TP4, slot J5A is abnormal, check matrix card at slot J4A; and if any other indications are abnormal, check matrix card at slot J10A.
10	Connect patch board test probe S12A to test point TP8A on 501051 unit. Press START DISPLAY switch S01.	TP2, J18A; and TP3, J17A.	int	6.6 microsecond true pulse each time S01 is pressed.	Checks K input to F/F09 and F/F10 respectively. If indication is abnormal, check matrix card at slot J19A.
11	Same as step 10	TP2, slot J17A; TP3, slot J16A; TP2, slot J16A; TP3, slot J14A; TP2, slot J14A; and TP3, slot J12A.	int	Same as step 10	Checks K input to F/F11–F/F16 respectively. If indication is abnormal, check matrix card at slot J15A.

Step	Procedure	Test point	Sync source	Normal indication	Remarks
12	Same as step 10	TP2, slot J12A; TP3, slot J11A; TP2, slot J11A; TP3, slot J8A; TP2, slot J8A; TP3, slot J9A; TP2, slot J9A; and TP3, slot J5A.	int	Same as step 10	Checks K input to F/F17–F/F24 respectively. If indication at TP3, slot J5A is abnormal, check matrix card at slot J4A and if any other indication is abnormal, check matrix card at slot J10A.

CHAPTER 7
ALIGNMENT AND ADJUSTMENT

This chapter contains alignment and adjustment information for the tracking computer test function and the digital data display function. Adjustment of these functions is accomplished by performing the respective initial switch operations. Initial switch operations for the tracking computer test function are contained in paragraph 49, and initial switch operations for the digital data display function are contained in paragraph 61. Operational tests are required before returning equipment to operation after the equipment has been repaired or if the equipment has been inoperative for any prolonged period. The tracking computer test function operation test is described in paragraph 51 and the digital data display function operational test is described in paragraph 63. Internal alignment of these circuits is not required.

APPENDIX
REFERENCES

A list of references applicable to this manual and available to field maintenance personnel is contained in TM 11-5840-271-30/1, Field (Third Echelon) Maintenance Manual, Processing Center, Radar Data OA-4333/MSQ-28B, Description, Data, and General Functional Theory (U).

GLOSSARY

Explanation of the abbreviations and definitions of unusual terms used in this manual are contained in the glossary of TM 11-5840-271-30/1 Field (Third Echelon) Maintenance Manual, Processing Center, Radar Data OA-4333/MSQ-28B, Description, Data, and General Functional Theory (U).

INDEX

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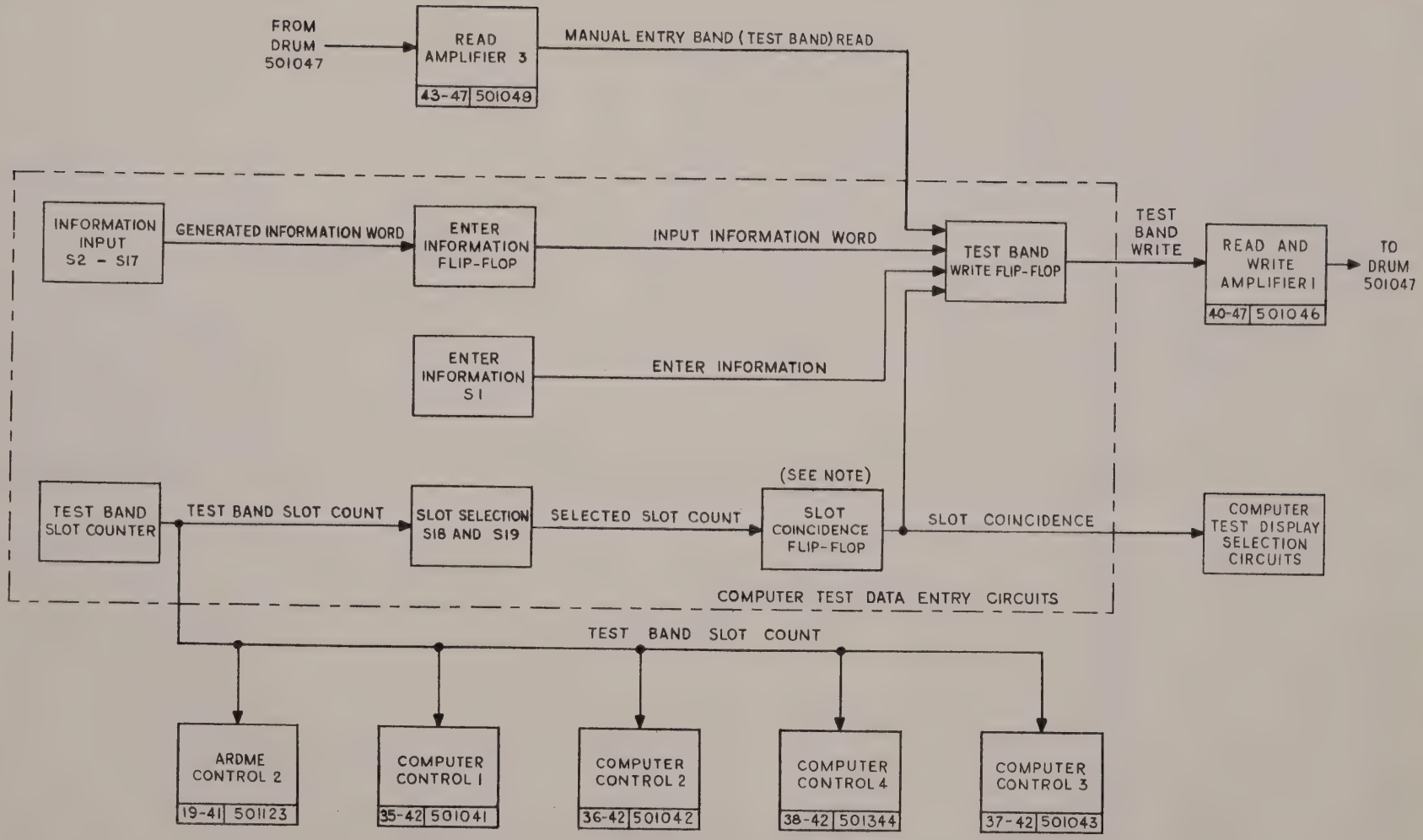


NOTE:
SLOT COINCIDENCE FLIP-FLOP IS LOCATED IN 501056 UNIT; ALL OTHER CIRCUITS ARE LOCATED IN 501051 UNIT.

TM5895-271-30-177

Figure 2. Computer test data entry, block diagram.

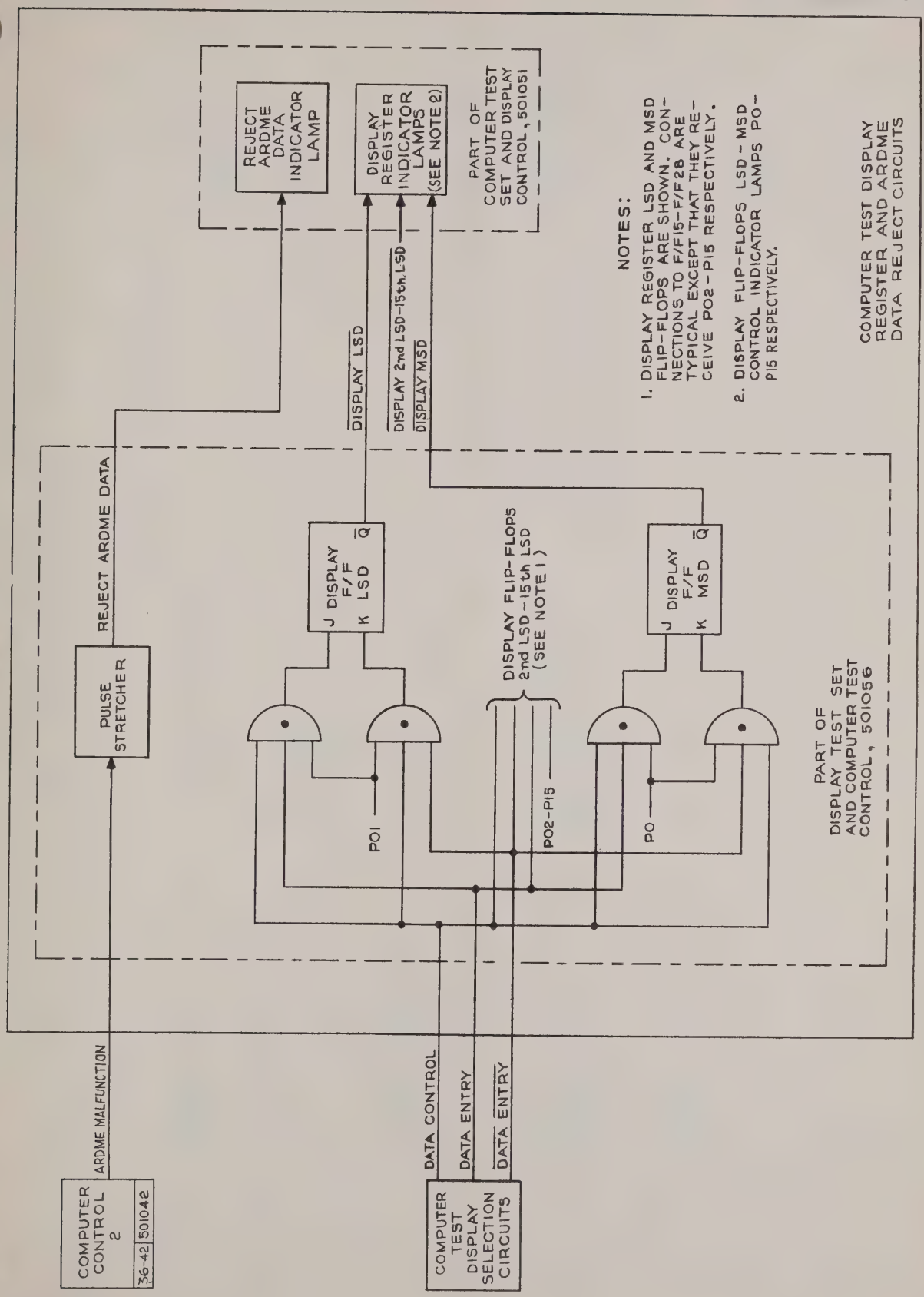


Figure 4. Computer test display register and ARDME data reject, block diagram.

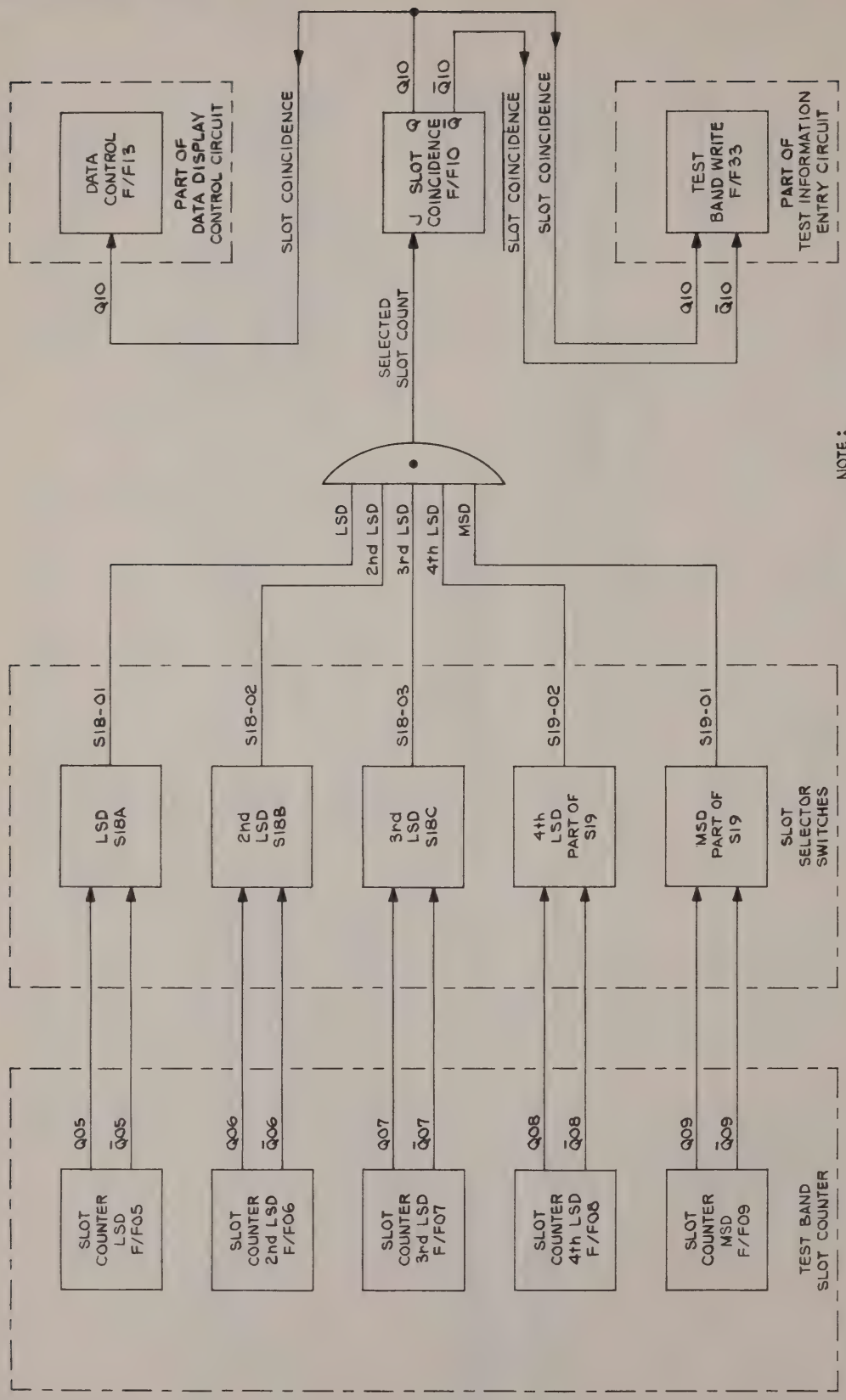


Figure 5. Slot selection circuit, block diagram.

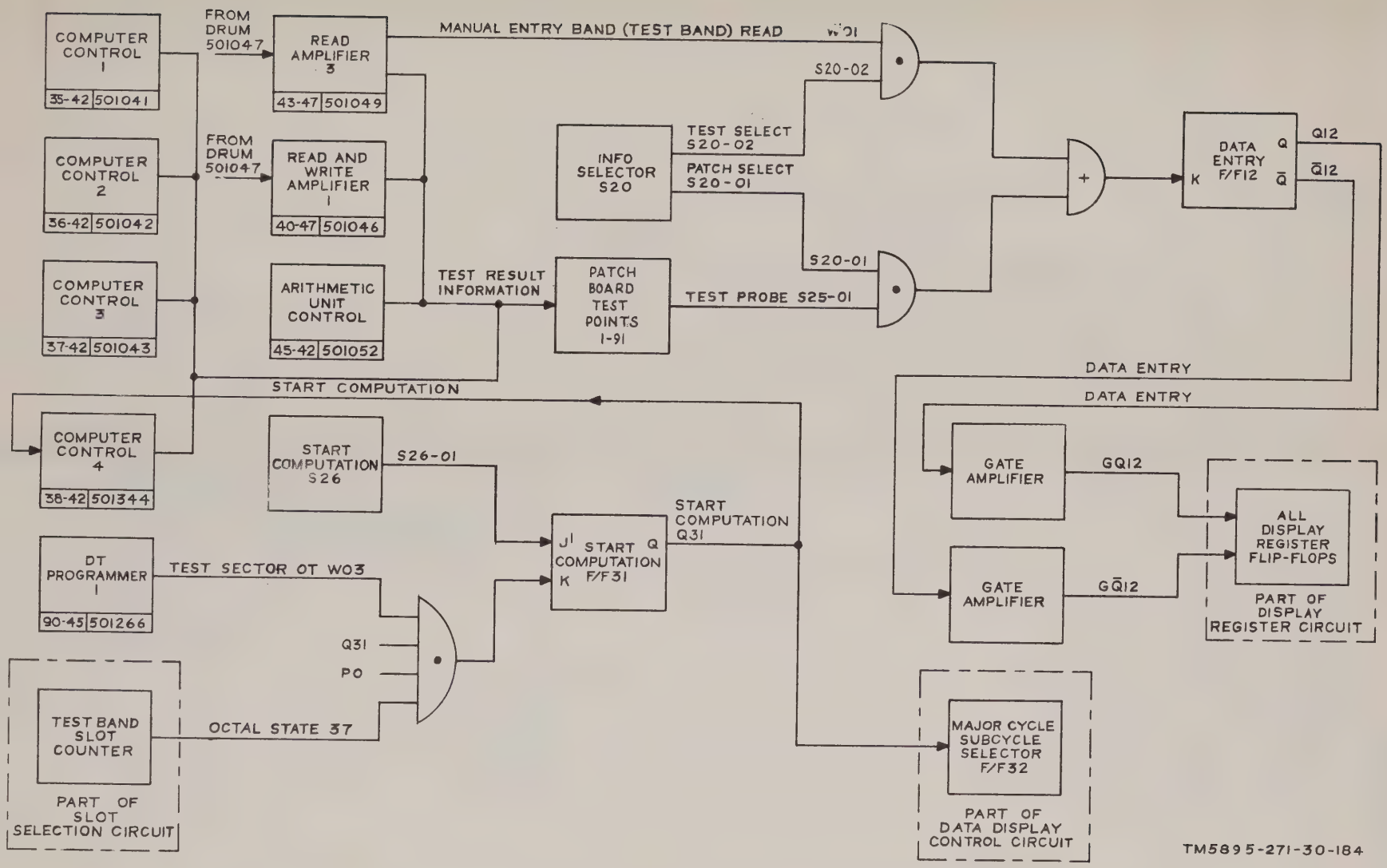


Figure 9. Display data entry circuit, block diagram.

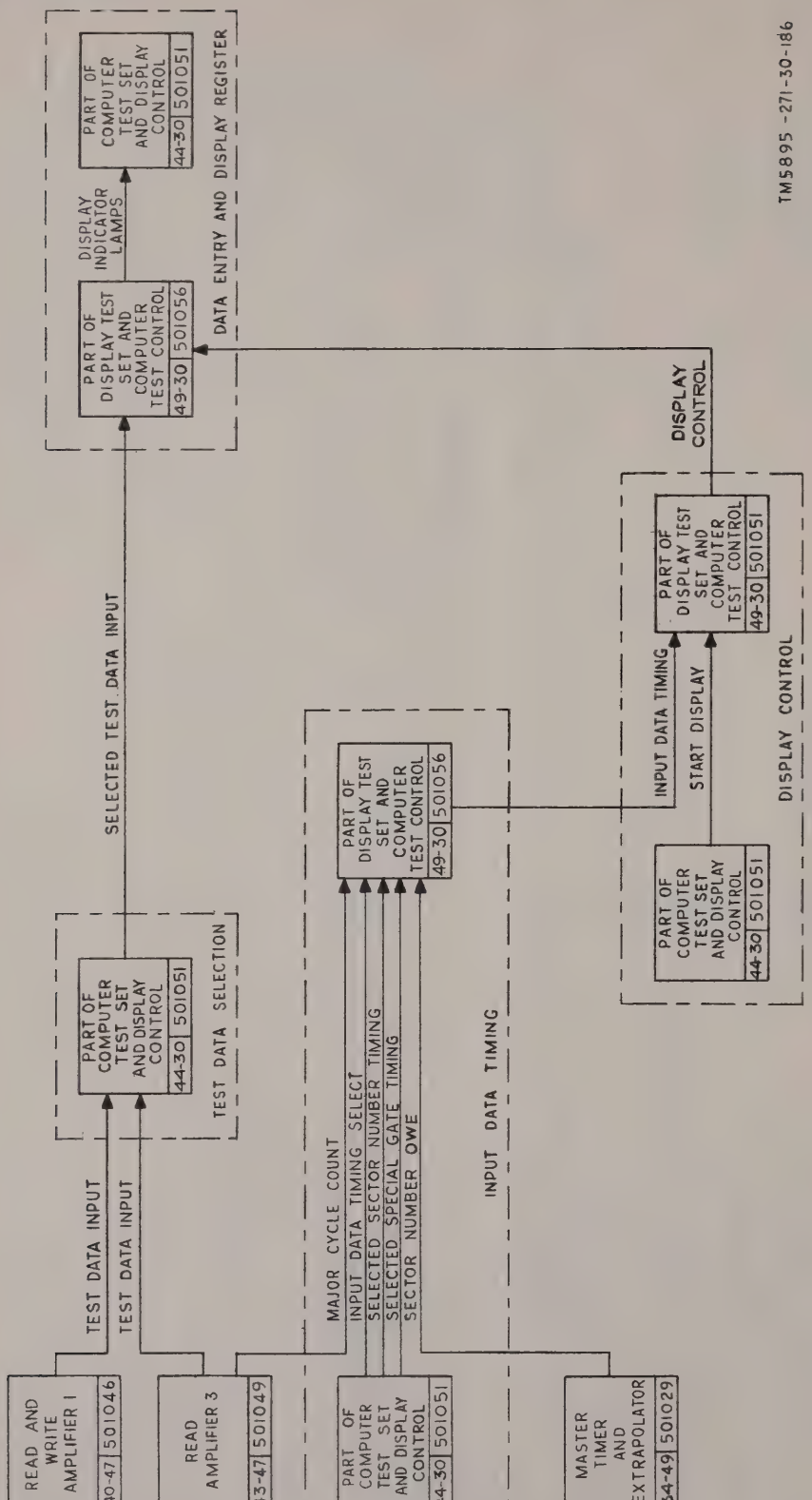


Figure 11. Digital data display function, block diagram.

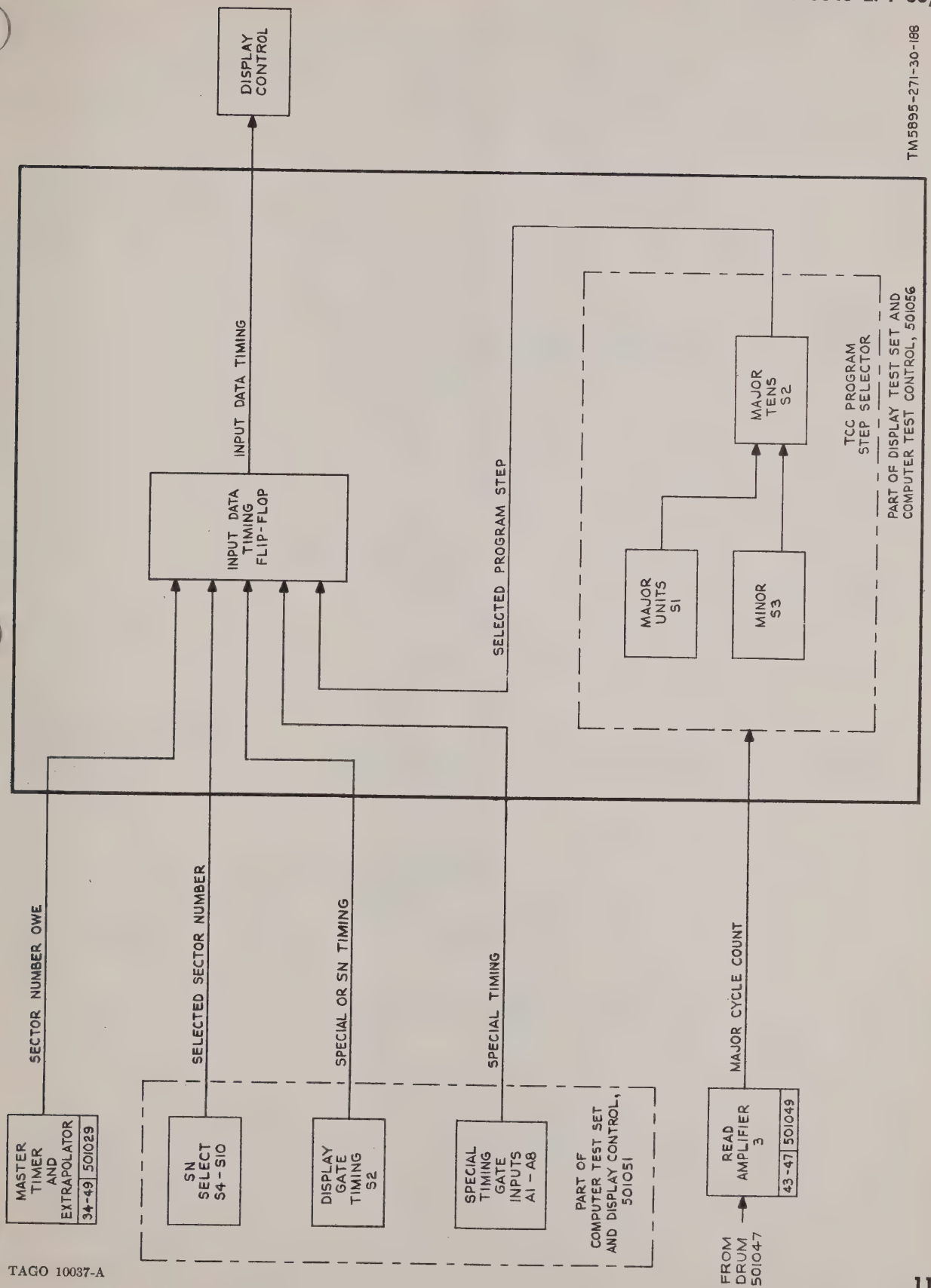


Figure 13. Input data timing, block diagram.

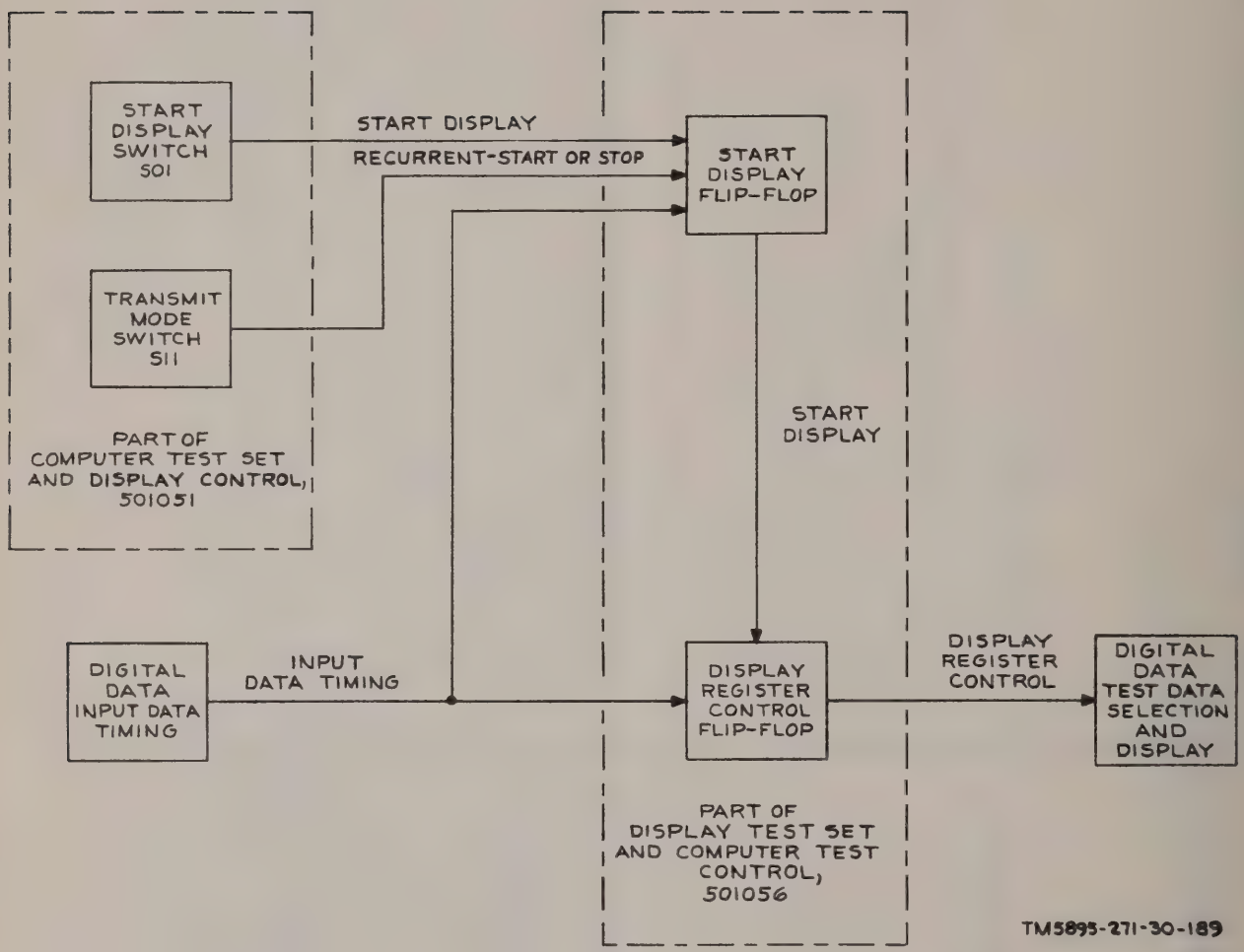


Figure 14. Display control, block diagram.

Figure 16. Data input circuit, block diagram.

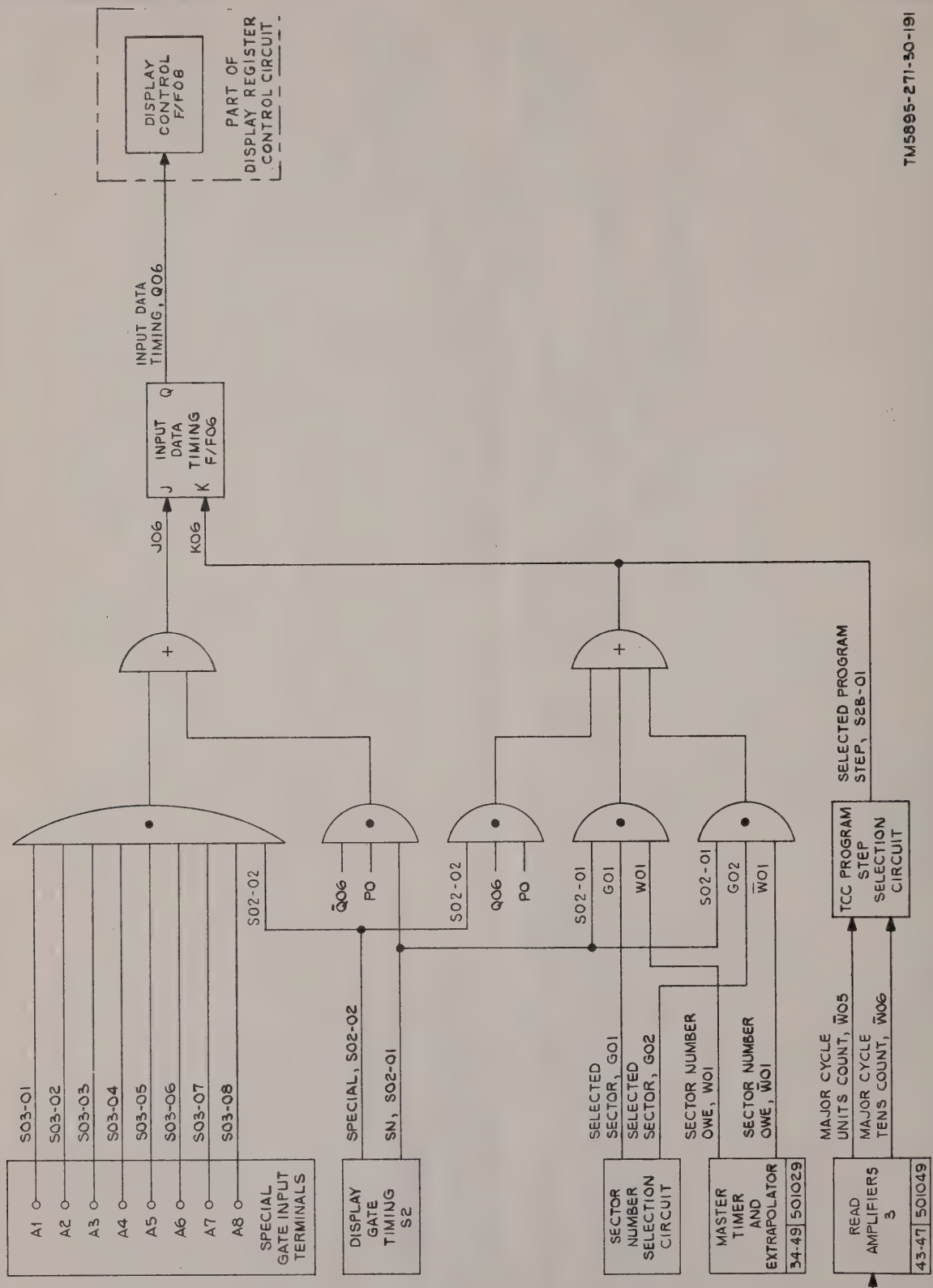


Figure 16. Timing circuits, block diagram.

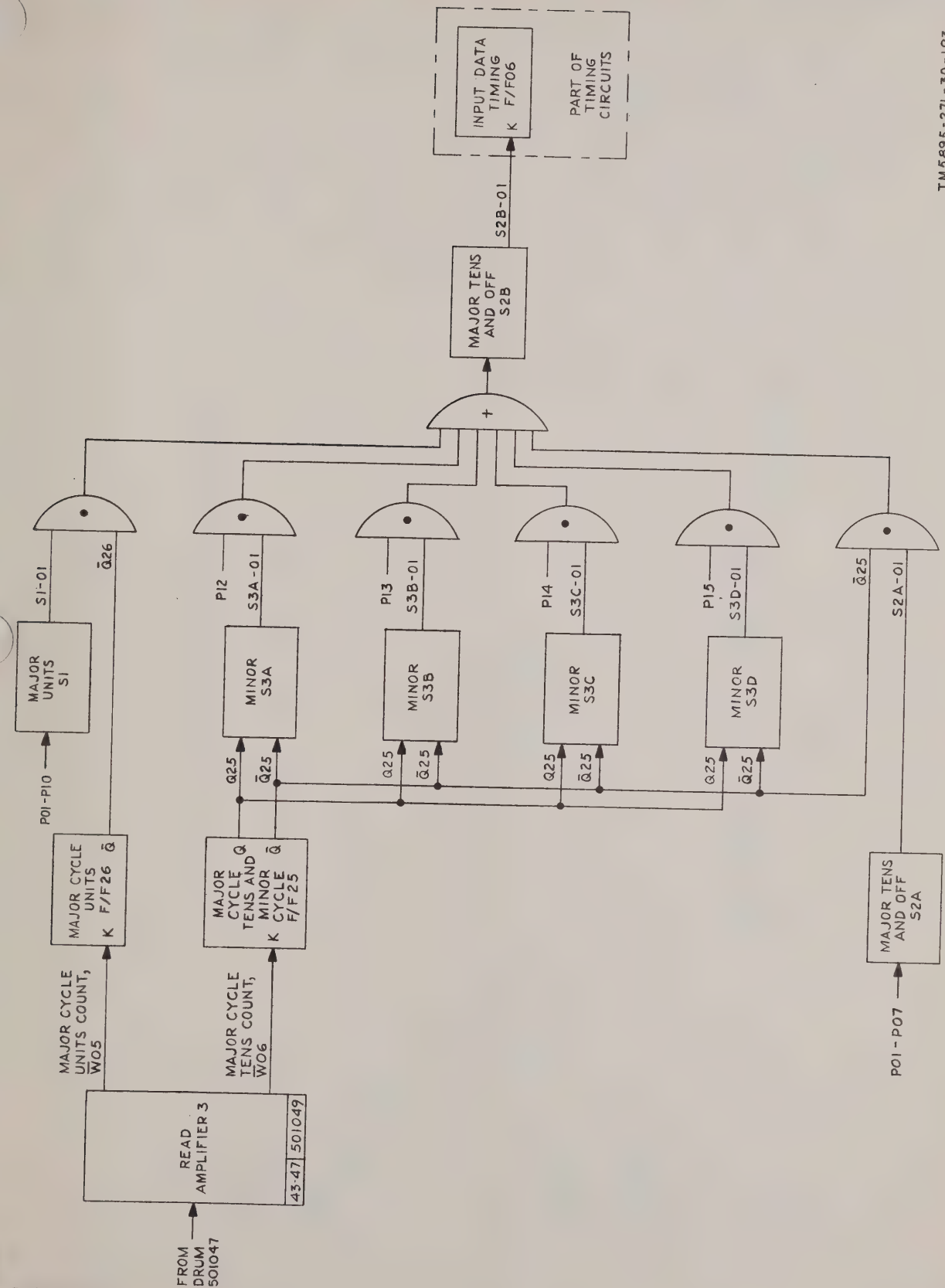


Figure 18. Program step selection circuit, block diagram.

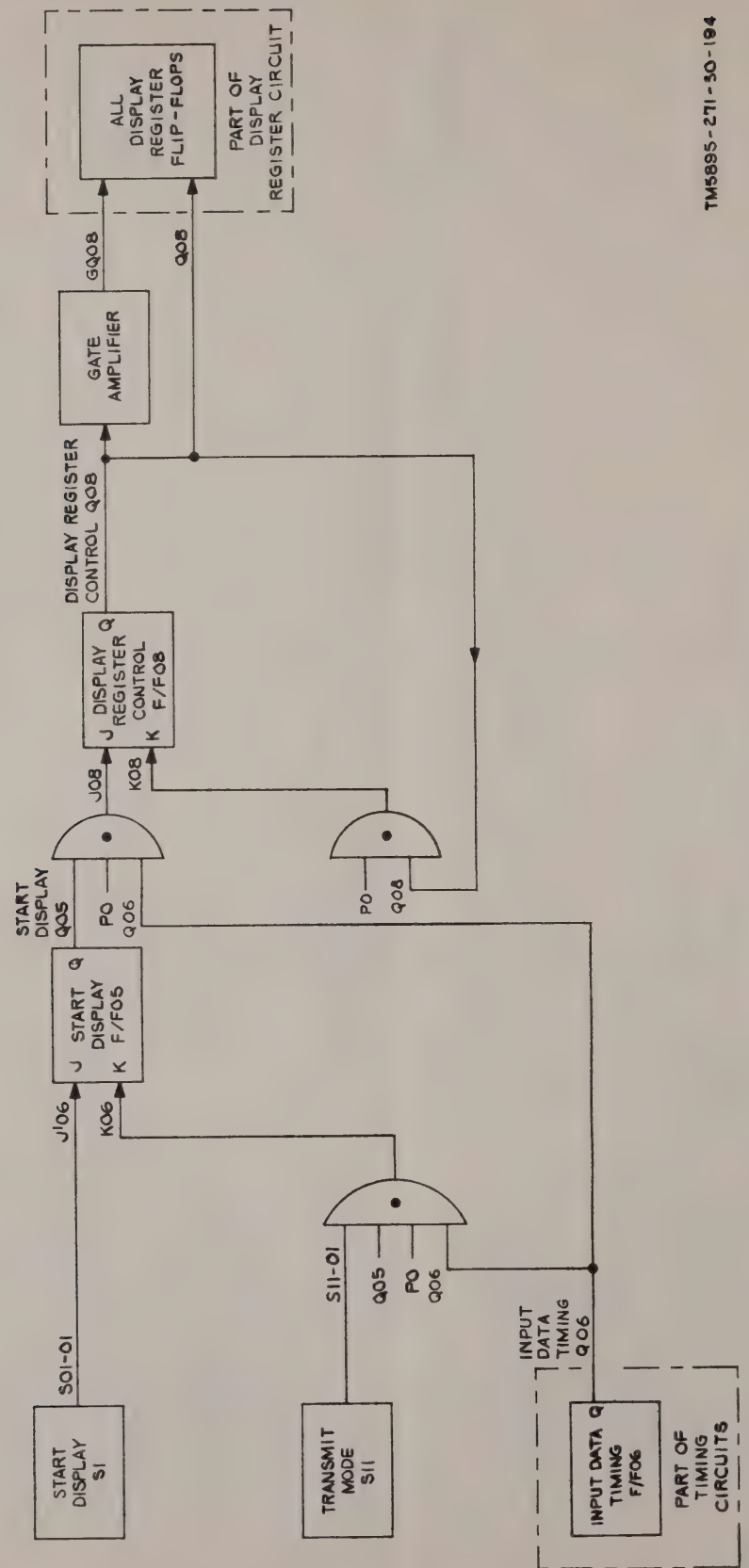


Figure 19. Display register control circuit, block diagram.

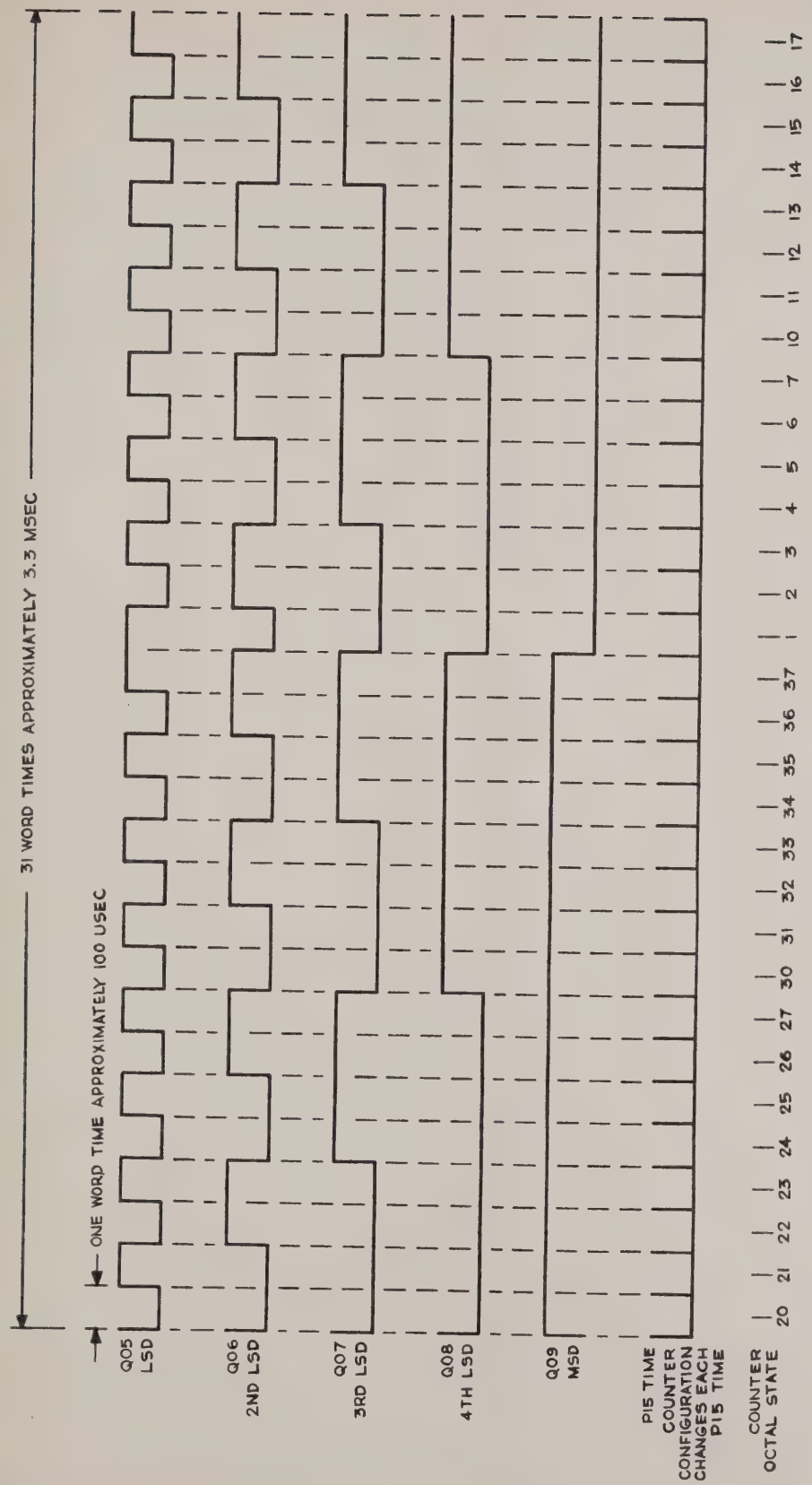
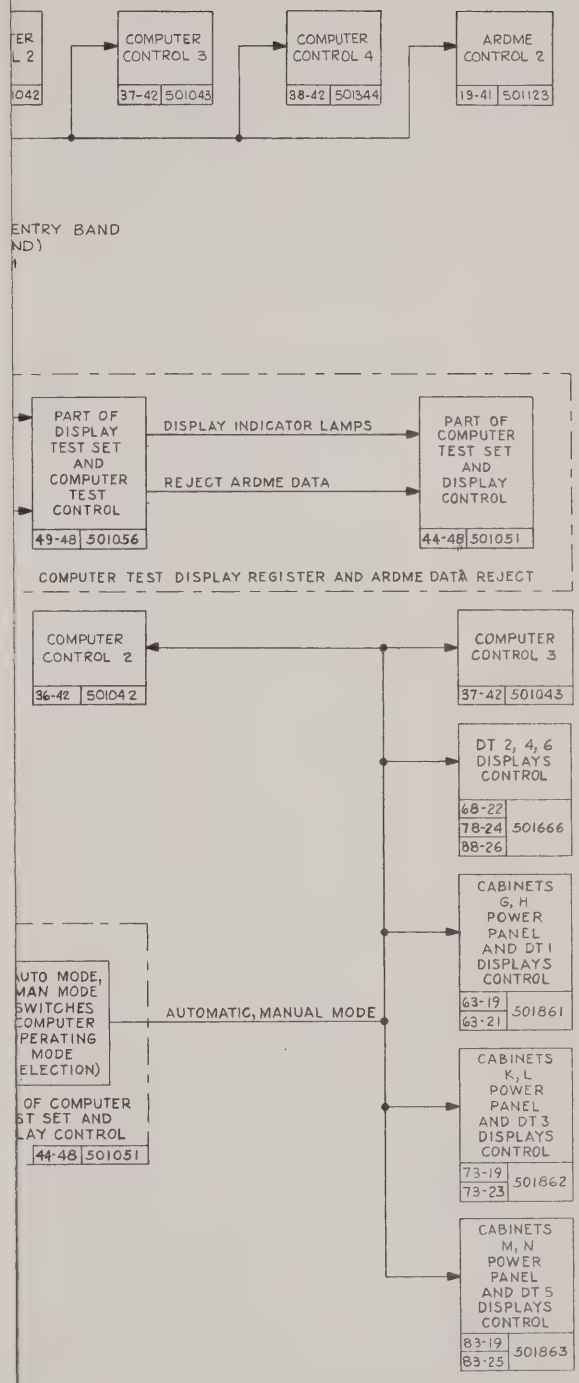


Figure 21. Test band slot counter, timing diagram.



TM5895-271-30-176

FIGURE 1

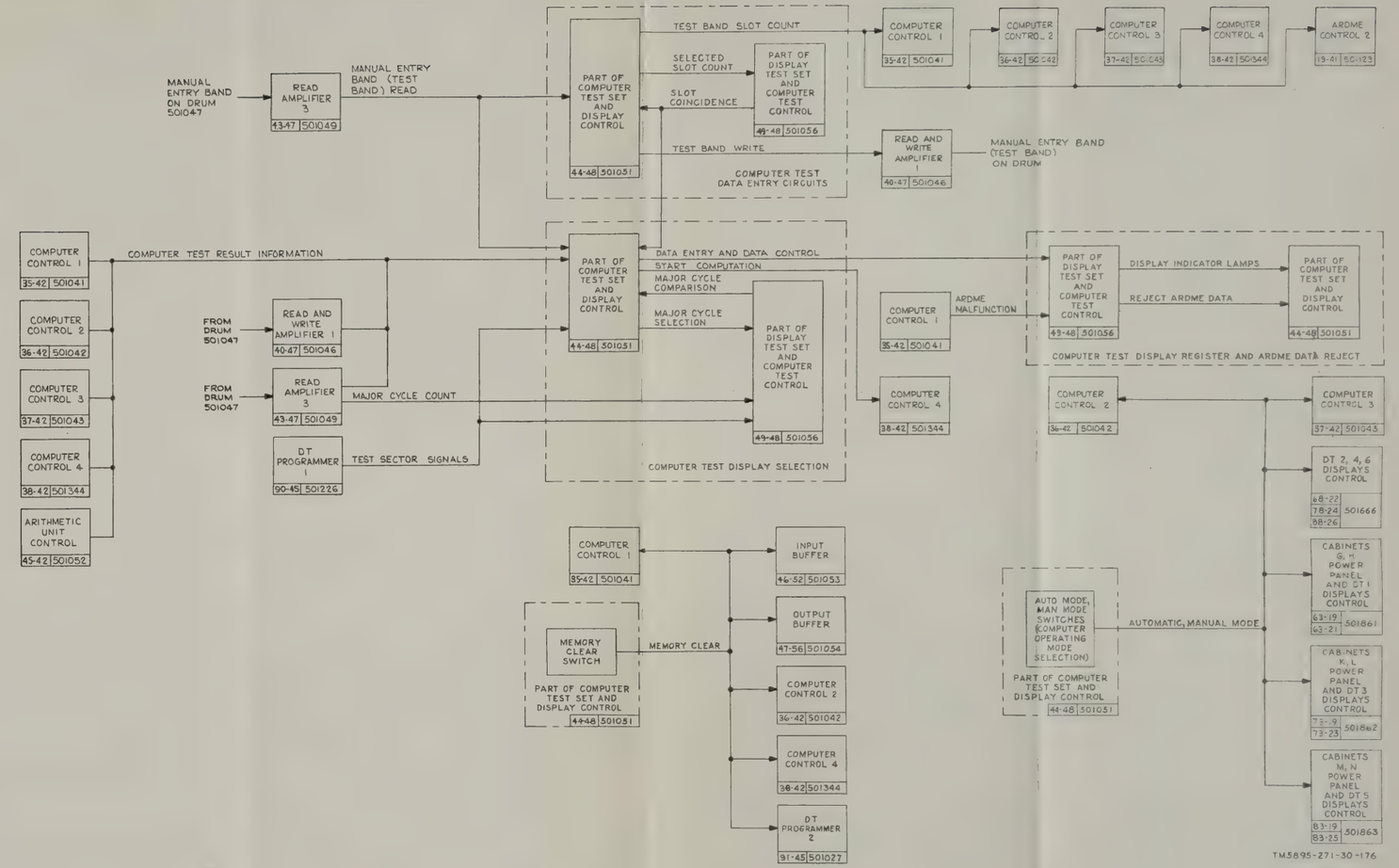
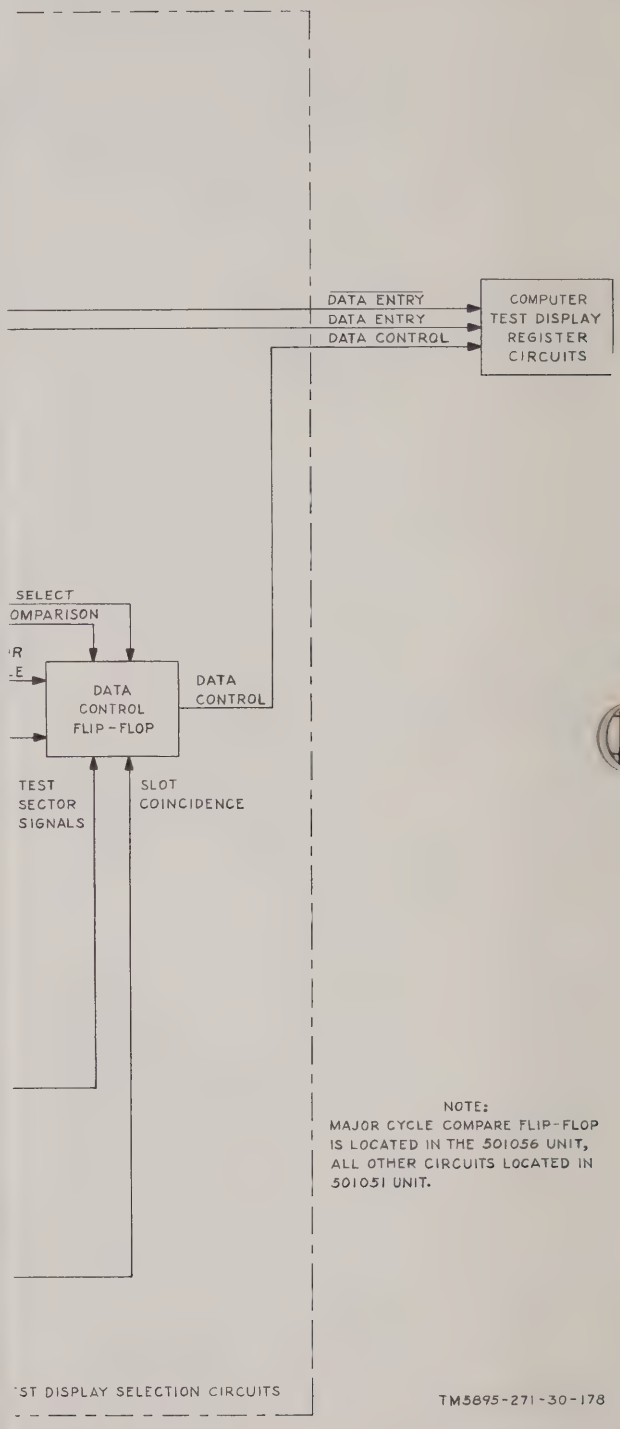


Figure 1. Tracking computer test function, block diagram.

FIGURE 1



TM5895-271-30-178

FIGURE 3

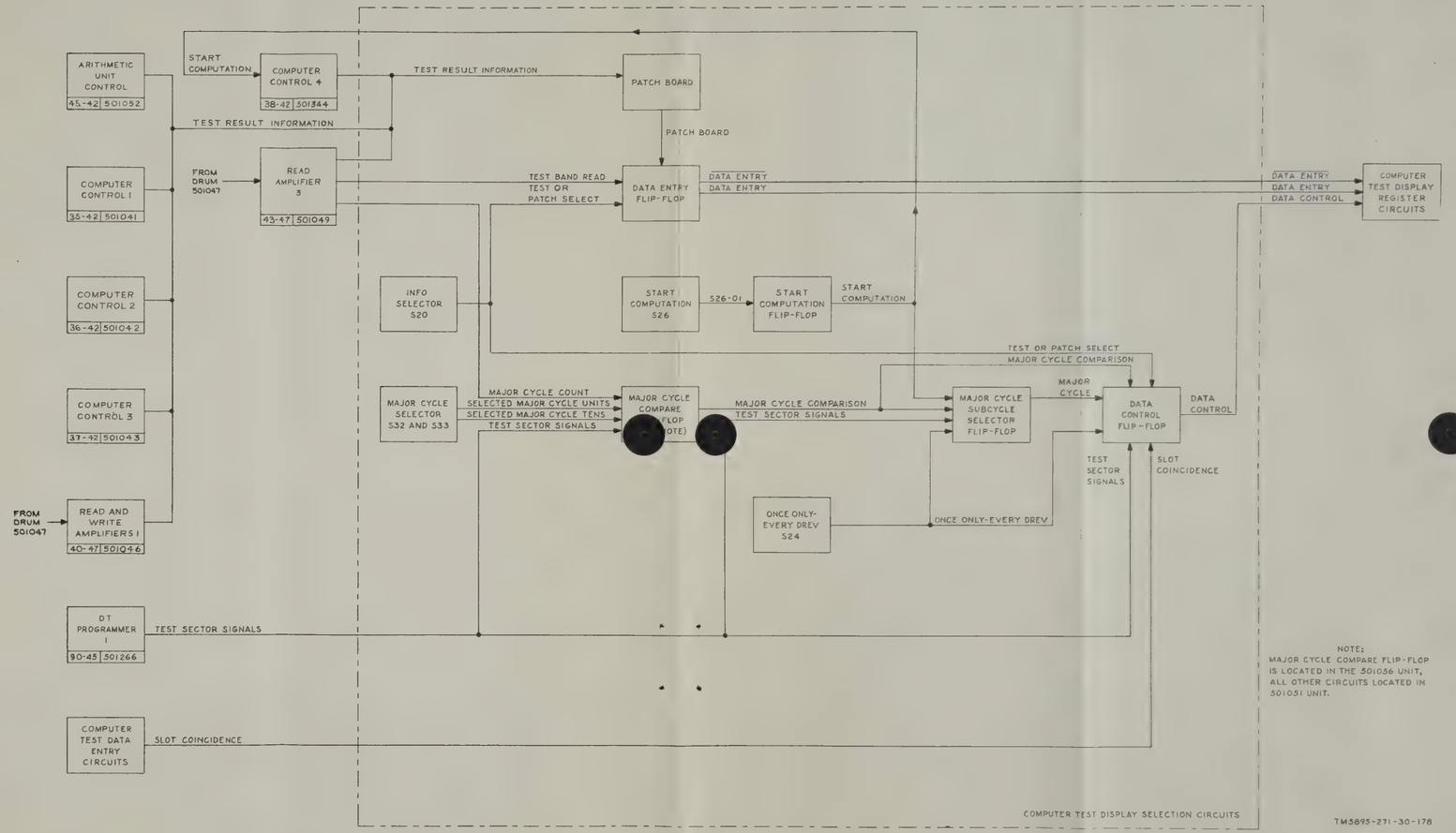
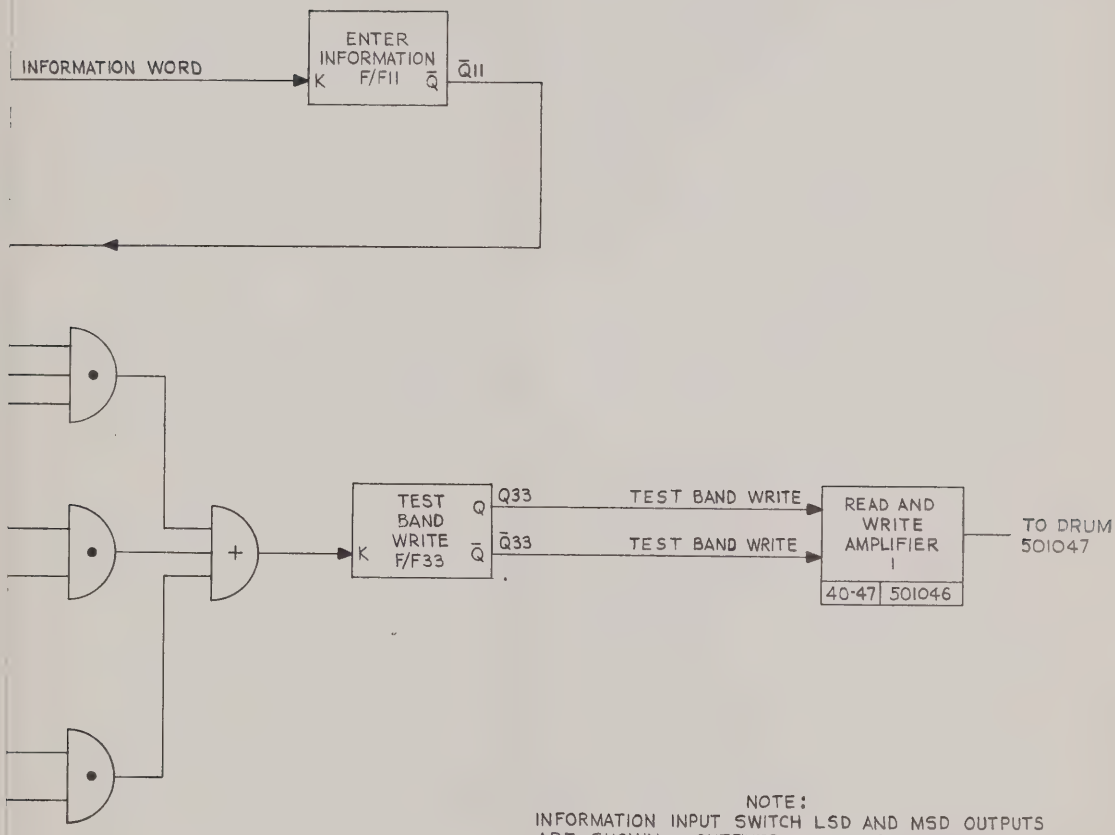


Figure 3. Computer test display selection, block diagram.

FIGURE 3



TM5895-271-30-181

Test information entry circuit, block diagram.

FIGURE 6

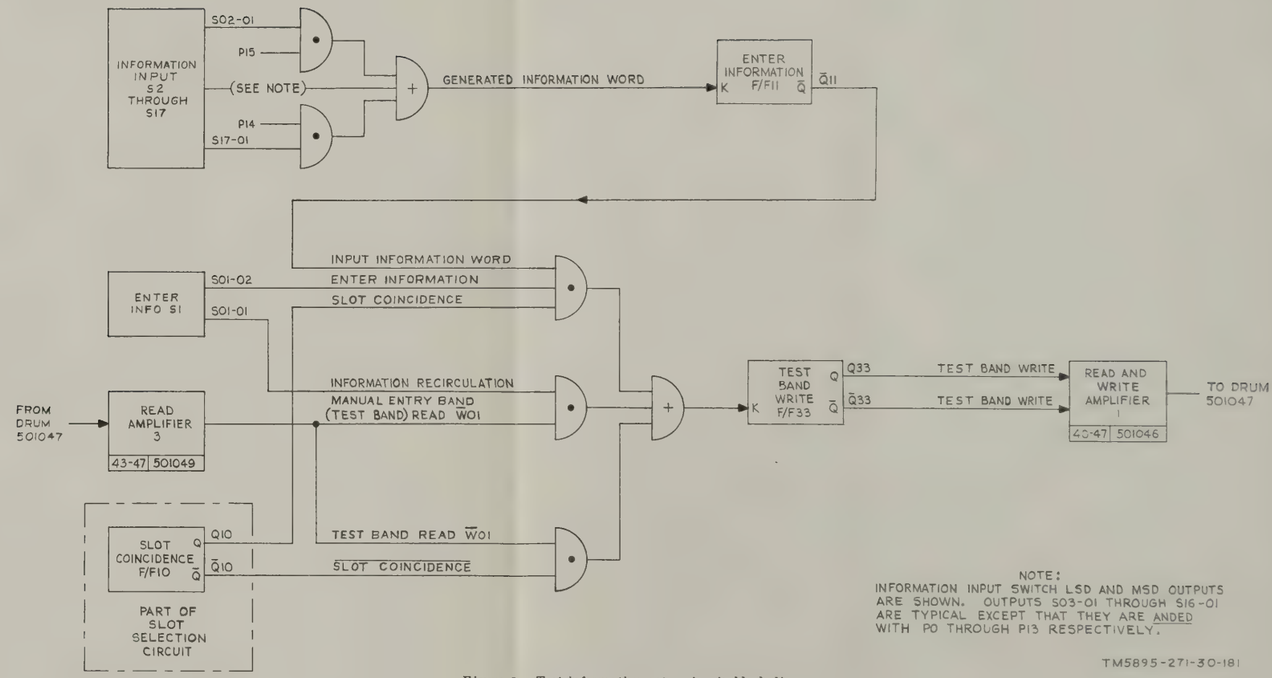
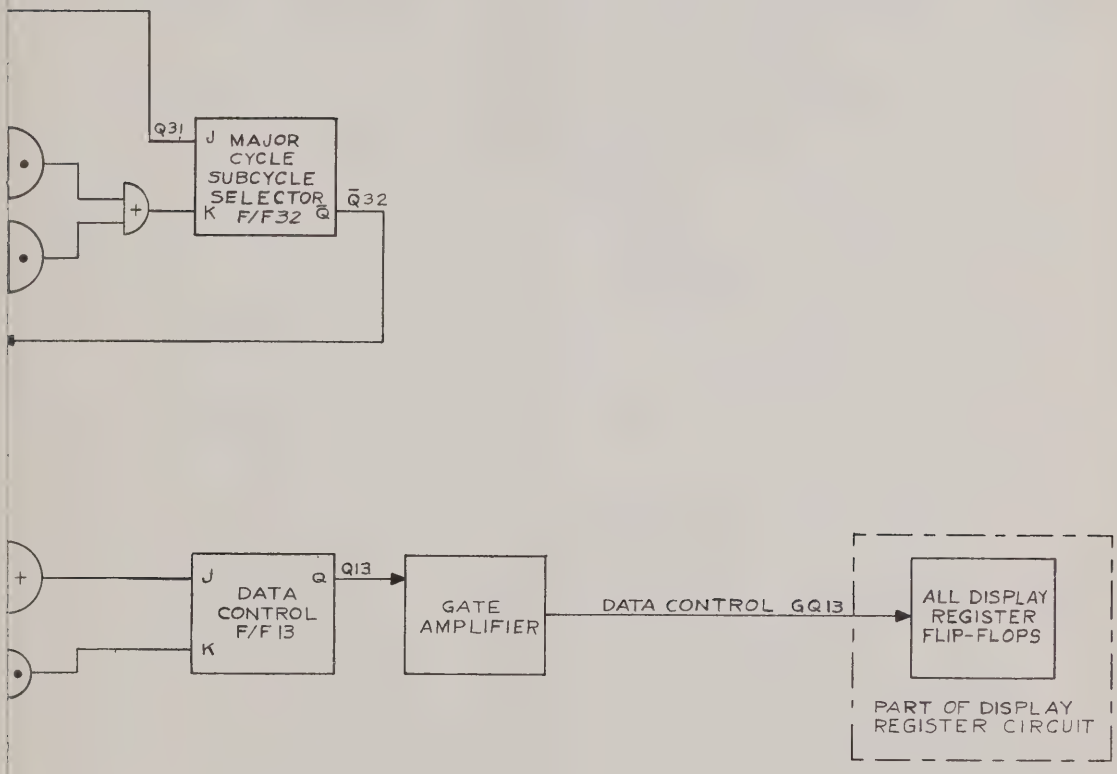


Figure 6. Test information entry circuit, block diagram.

FIGURE 6



TM5895-271-30-182

play control circuit, block diagram.

FIGURE 7

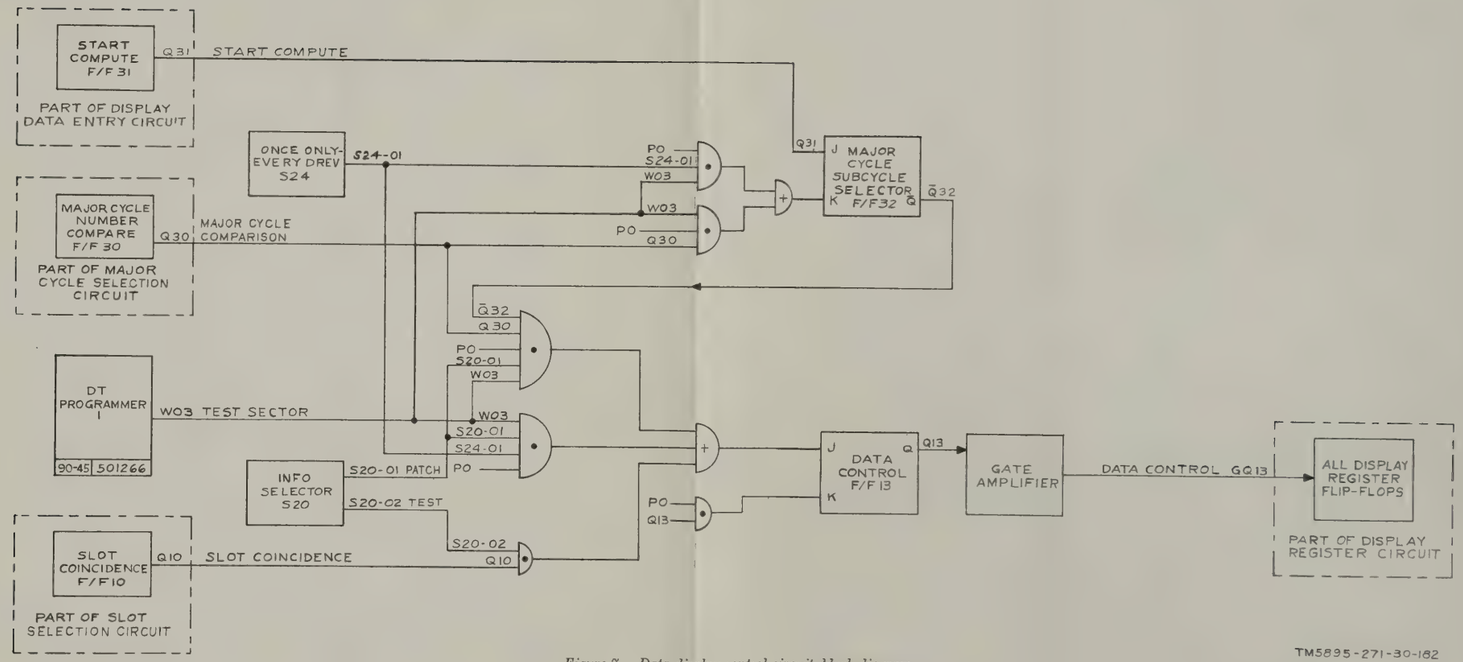


Figure 7. Data display control circuit, block diagram.

TM5895-271-30-182

FIGURE 7

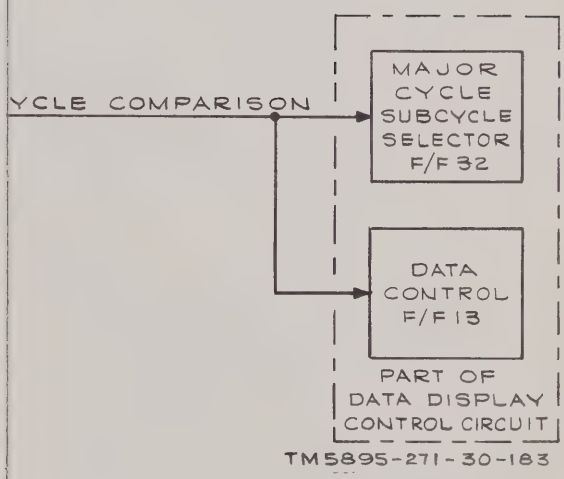

YCLE COMPARISON
MAJOR CYCLE SUBCYCLE SELECTOR F/F 32
DATA CONTROL F/F 13
PART OF DATA DISPLAY CONTROL CIRCUIT
TM5895-271-30-183

FIGURE 8

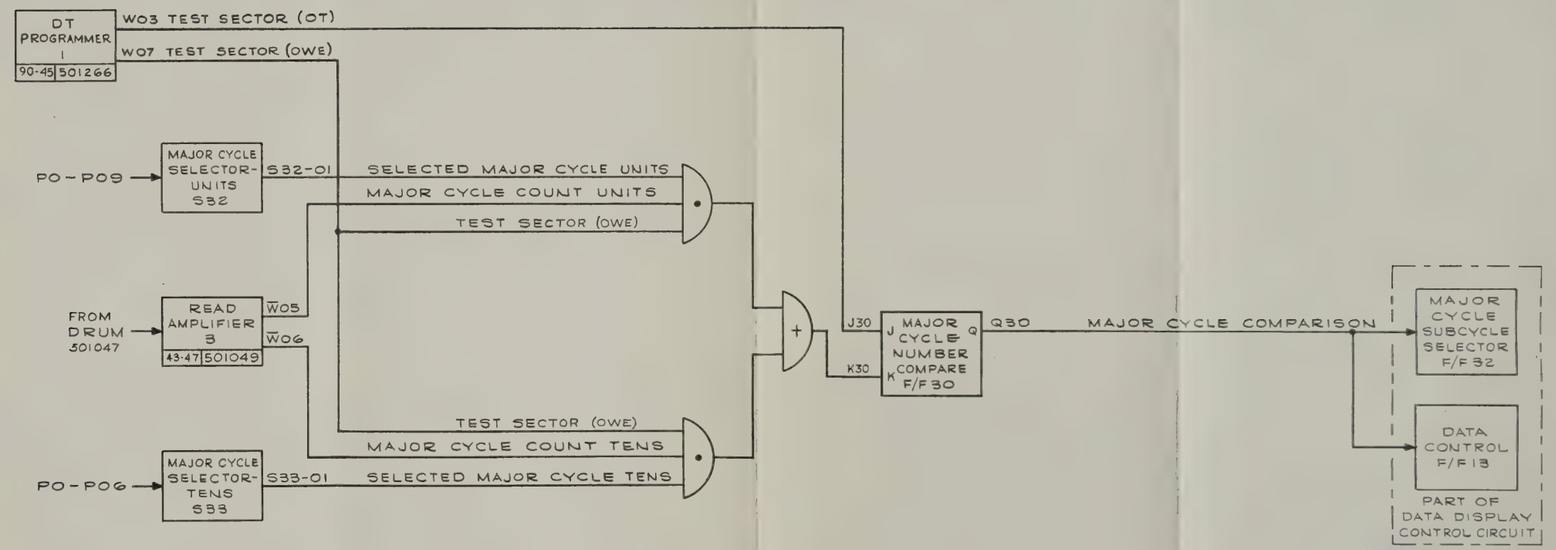
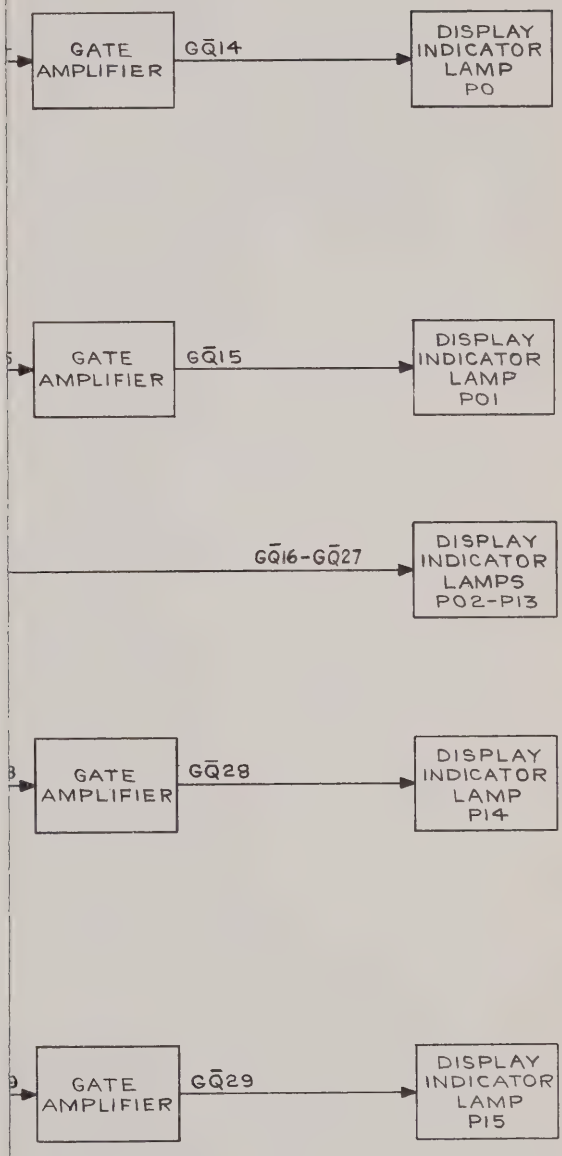


Figure 8. Major cycle selection circuit, block diagram.

FIGURE 8



NOTE:

CONNECTIONS TO 3rd LSD F/F16 THROUGH 14th LSD F/F27 ARE TYPICAL EXCEPT THAT THEY RECEIVE P TIMES P03 – P14 AND CONTROL DISPLAY INDICATOR LAMPS P02 - P13 RESPECTIVELY.

TM5895-271-30-185

FIGURE 10

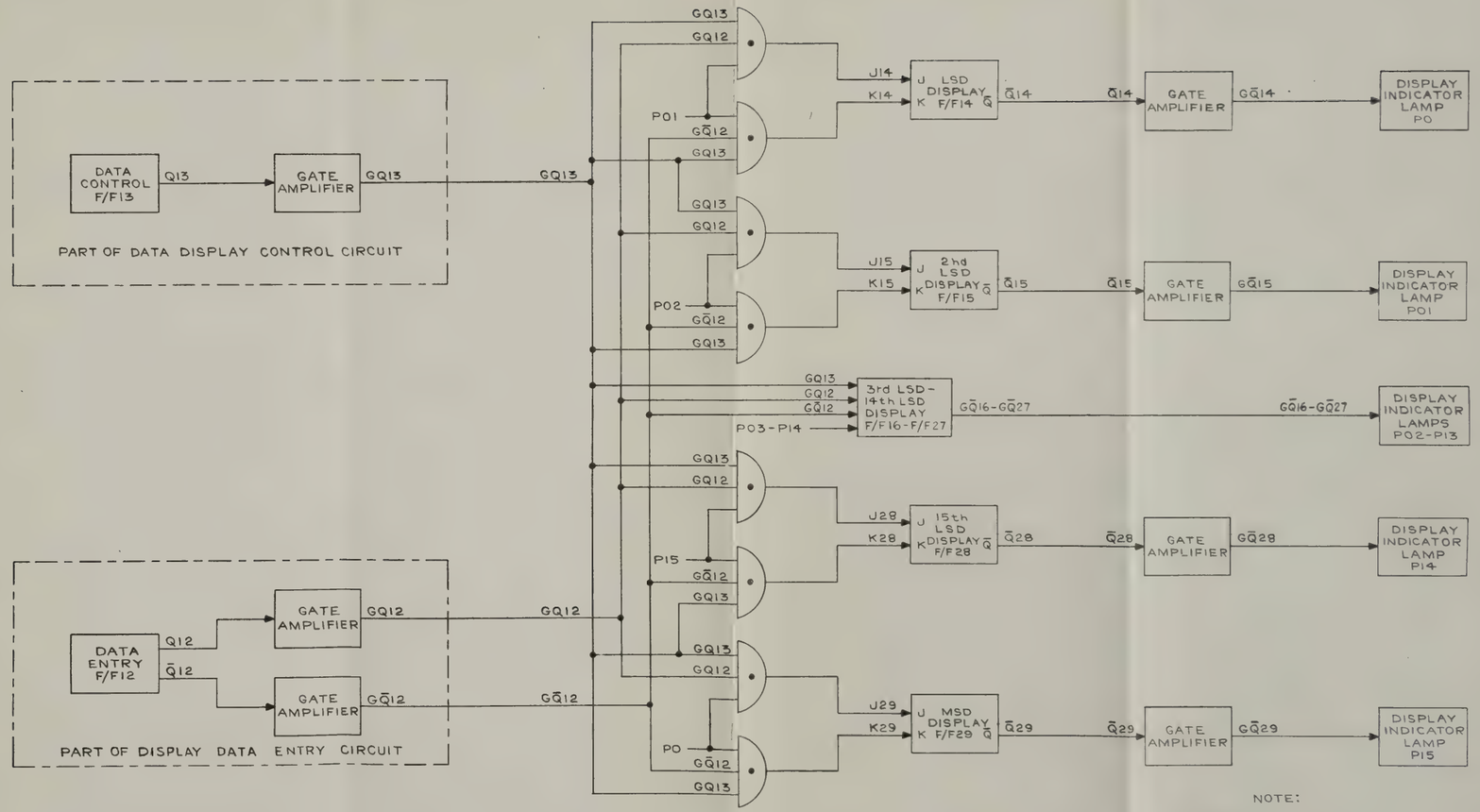
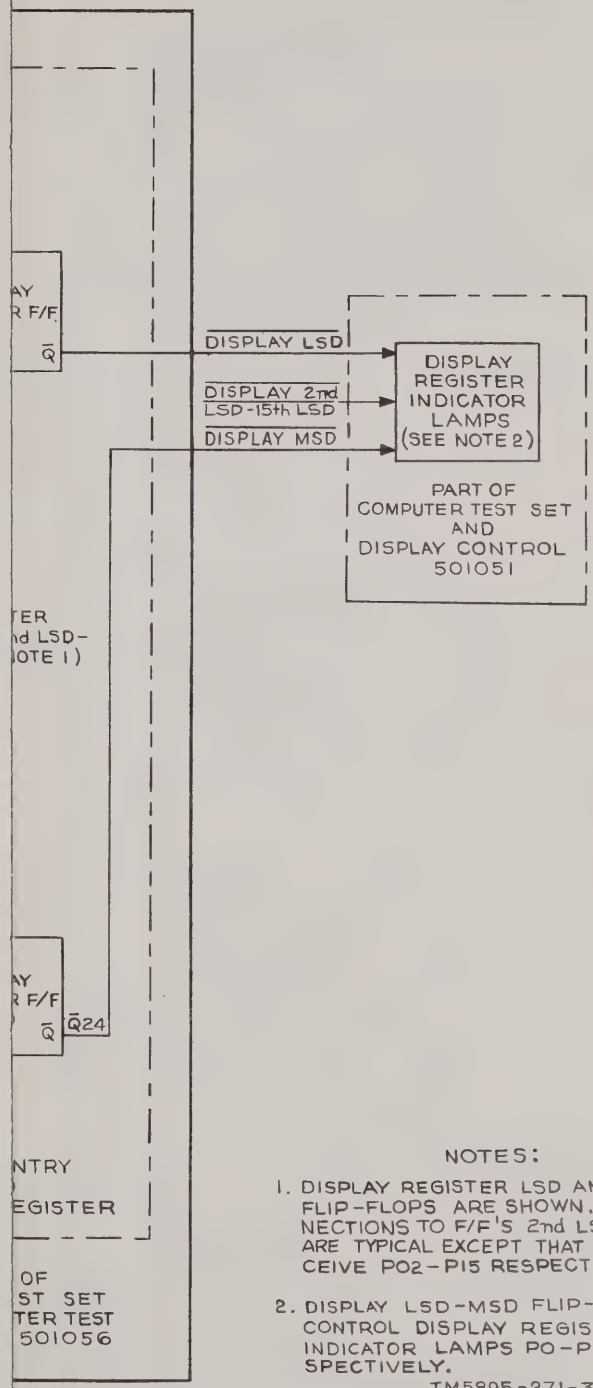


Figure 10. Computer test display register circuit, block diagram.

FIGURE 10



NOTES:

1. DISPLAY REGISTER LSD AND MSD FLIP-FLOPS ARE SHOWN. CONNECTIONS TO F/F'S 2nd LSD-15th LSD ARE TYPICAL EXCEPT THAT THEY RECEIVE P02-P15 RESPECTIVELY.
2. DISPLAY LSD-MSD FLIP-FLOPS CONTROL DISPLAY REGISTER INDICATOR LAMPS P0-P15 RESPECTIVELY.

TM5895-271-30-187

FIGURE 12

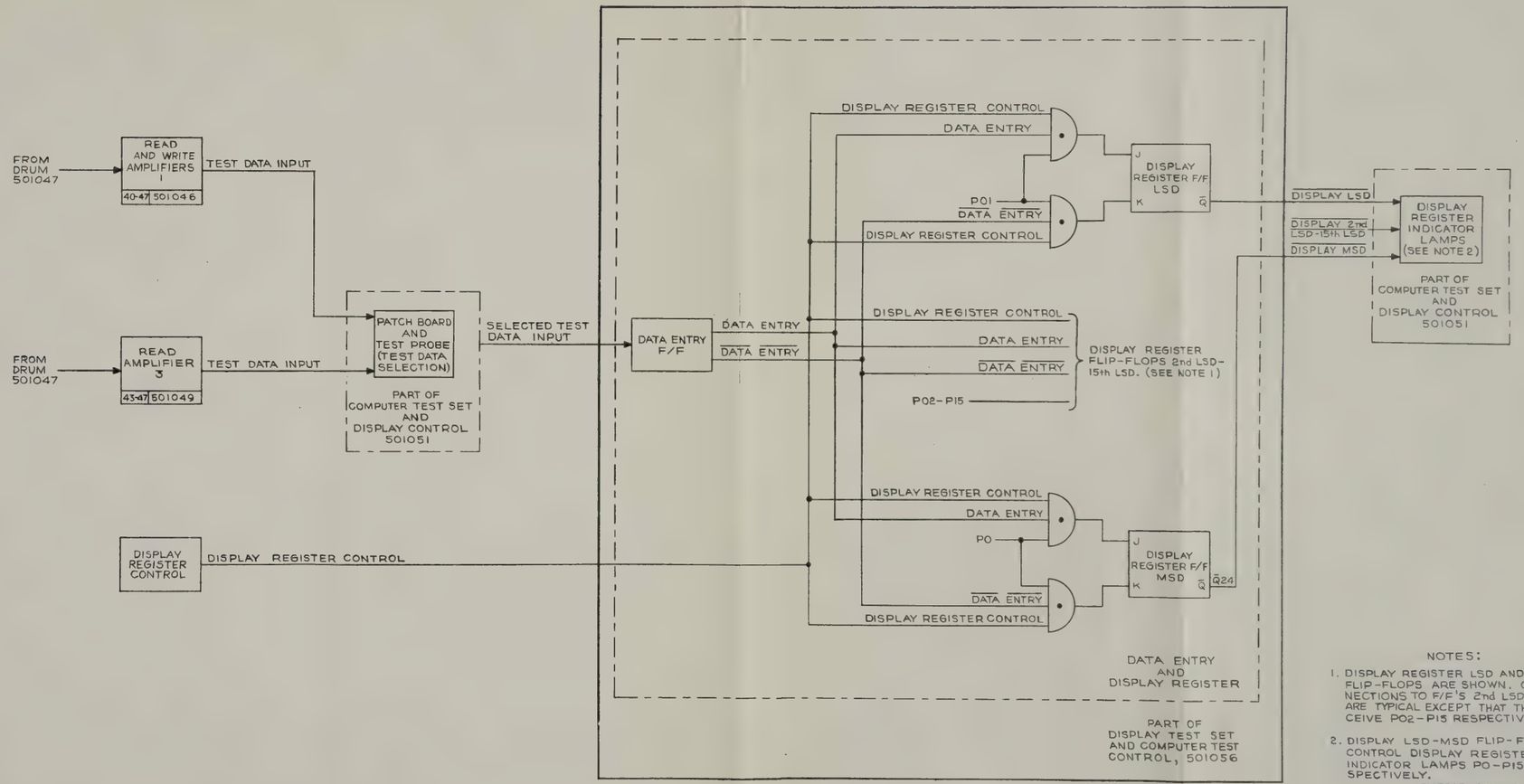
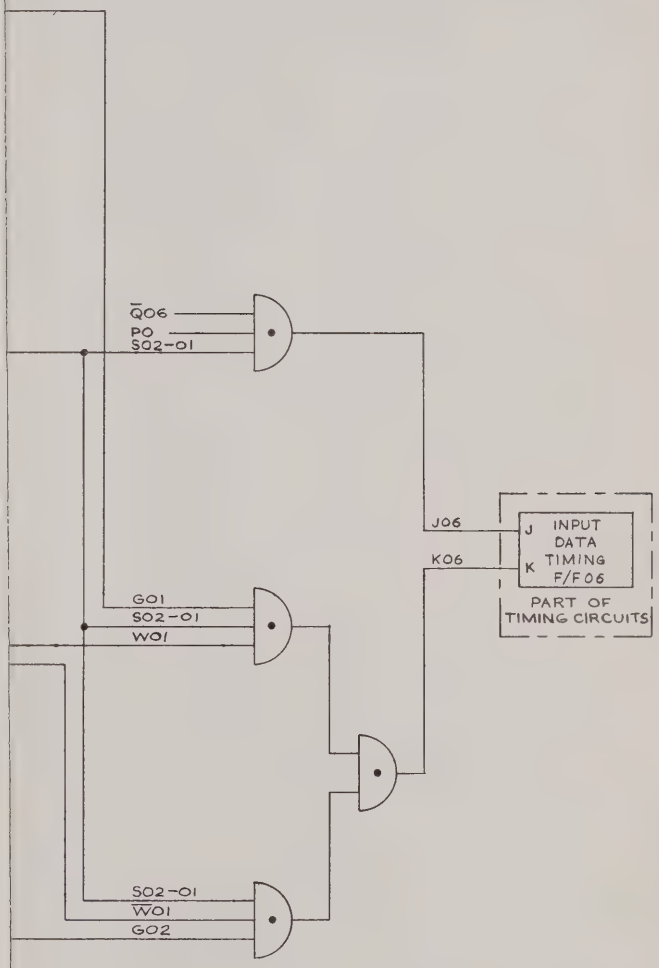


Figure 12. Test data selection and display, block diagram.

FIGURE 12



TM5895-271-30-192

FIGURE 17

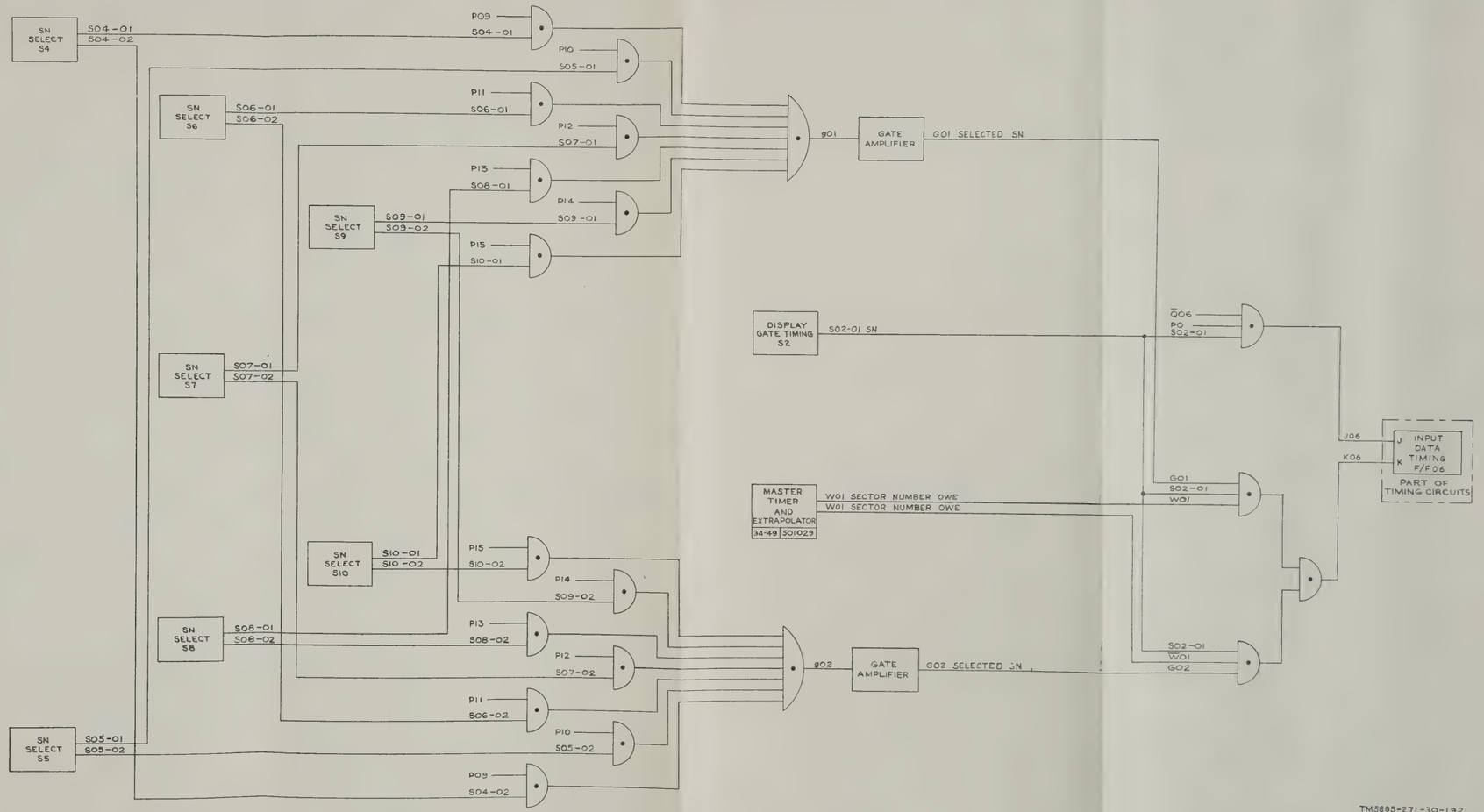
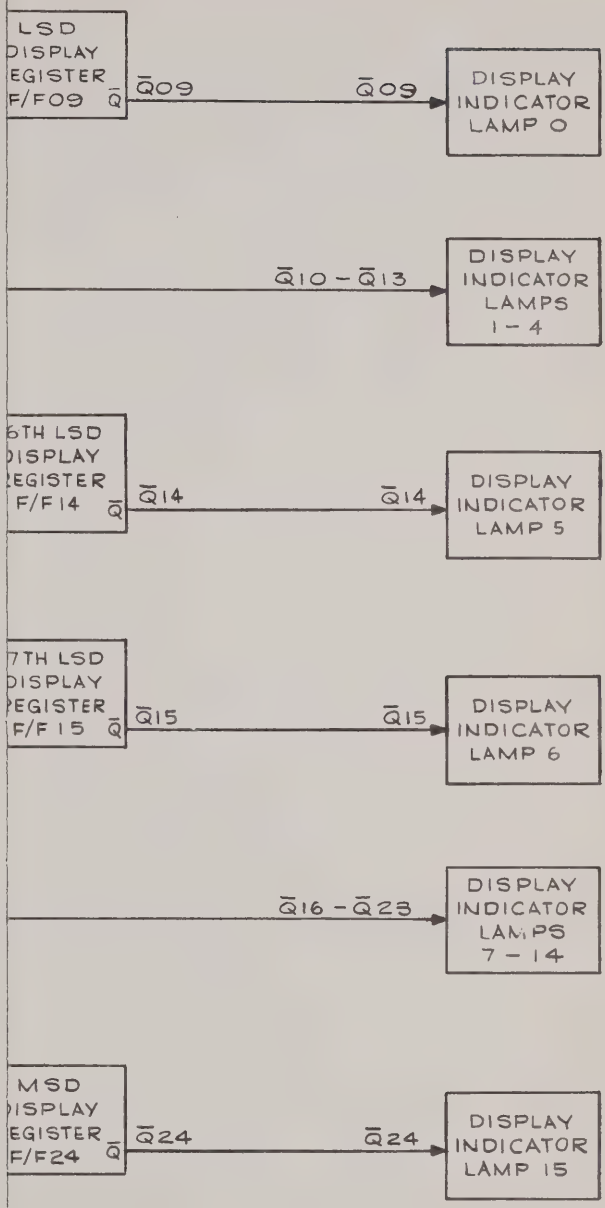


Figure 17. Sector number selection circuit, block diagram.

TM5895-271-30-192

FIGURE 17



OTES:

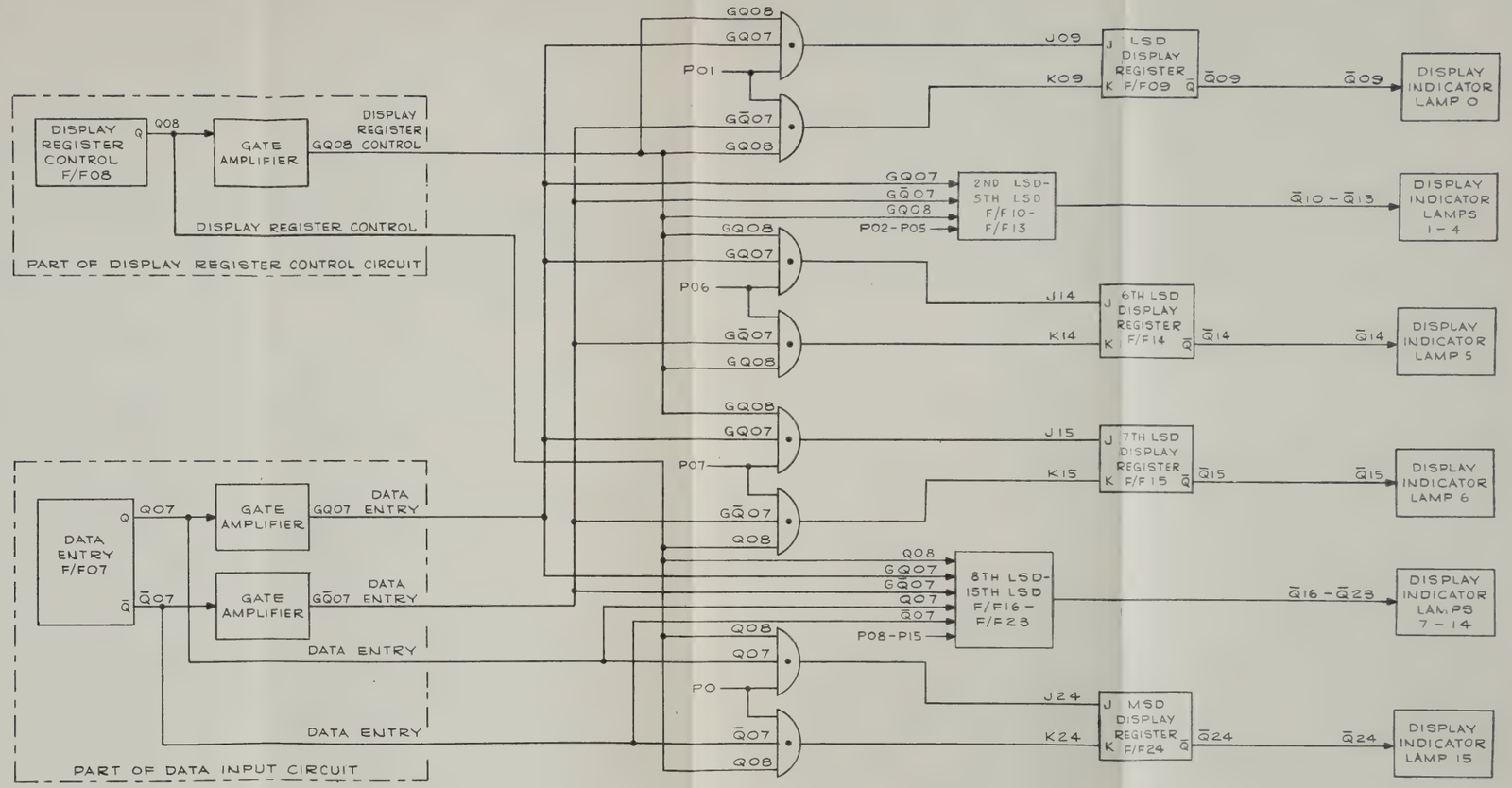
ATES OF F/F09 THROUGH F/F14
OF F/F15 AND K INPUT GATE OF F/F16.
THER INPUT GATES.

LIED TO INPUT GATES OF F/F09
D $\bar{Q}$07 ARE APPLIED TO INPUT GATES
.

CONSECUTIVE P TIMES FROM P01 THROUGH
S 0 THROUGH 15 RESPECTIVELY.

TM5895-271-30-195

FIGURE 20



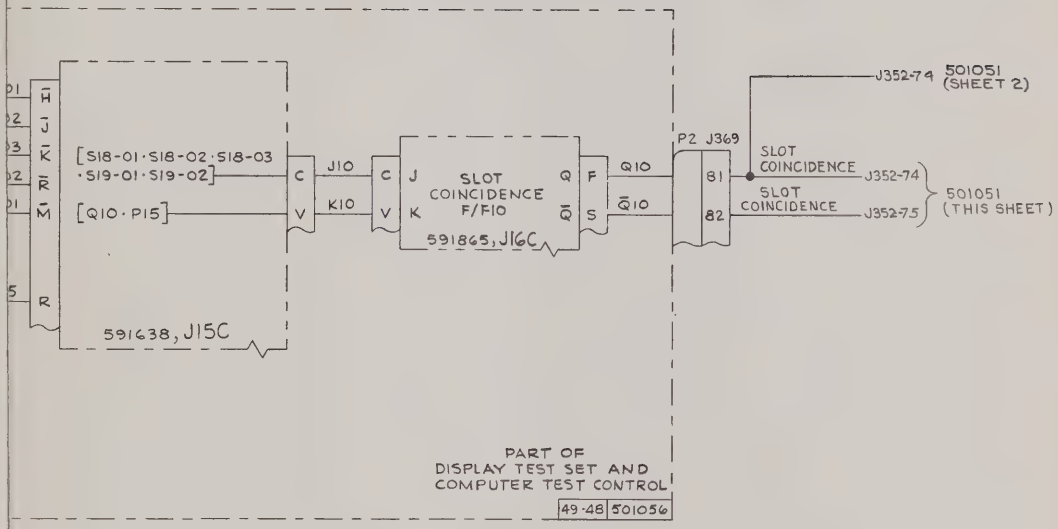
NOTES:

1. GQ08 IS APPLIED TO INPUT GATES OF F/F09 THROUGH F/F14 AND ALSO TO J INPUT GATE OF F/F15 AND K INPUT GATE OF F/F16. Q08 IS APPLIED TO ALL OTHER INPUT GATES.
2. GQ07 AND G$\bar{Q}$07 ARE APPLIED TO INPUT GATES OF F/F09 THROUGH F/F19. Q07 AND $\bar{Q}$07 ARE APPLIED TO INPUT GATES OF F/F20 THROUGH F/F24.
3. F/F09 THROUGH F/F24 RECEIVE CONSECUTIVE P TIMES FROM P01 THROUGH P0 AND CONTROL INDICATOR LAMPS 0 THROUGH 15 RESPECTIVELY.

Figure 20. Digital data display register circuit, block diagram.

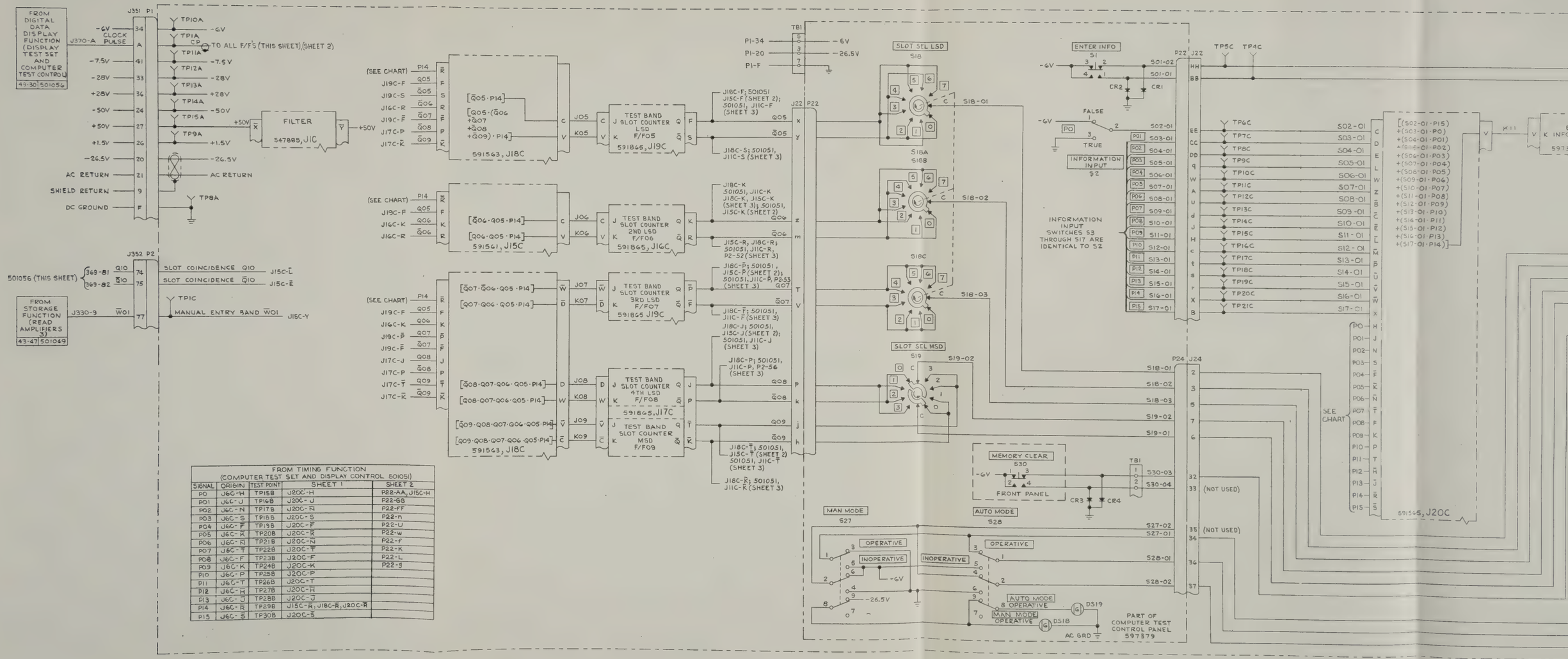
TM 5895-271-30-195

FIGURE 20



AY CONTROLS REFERENCE CHART		
L	REFERENCE NO.	JACK MATED WITH P3
	68-22	J453
	78-24	J553
	88-26	J653

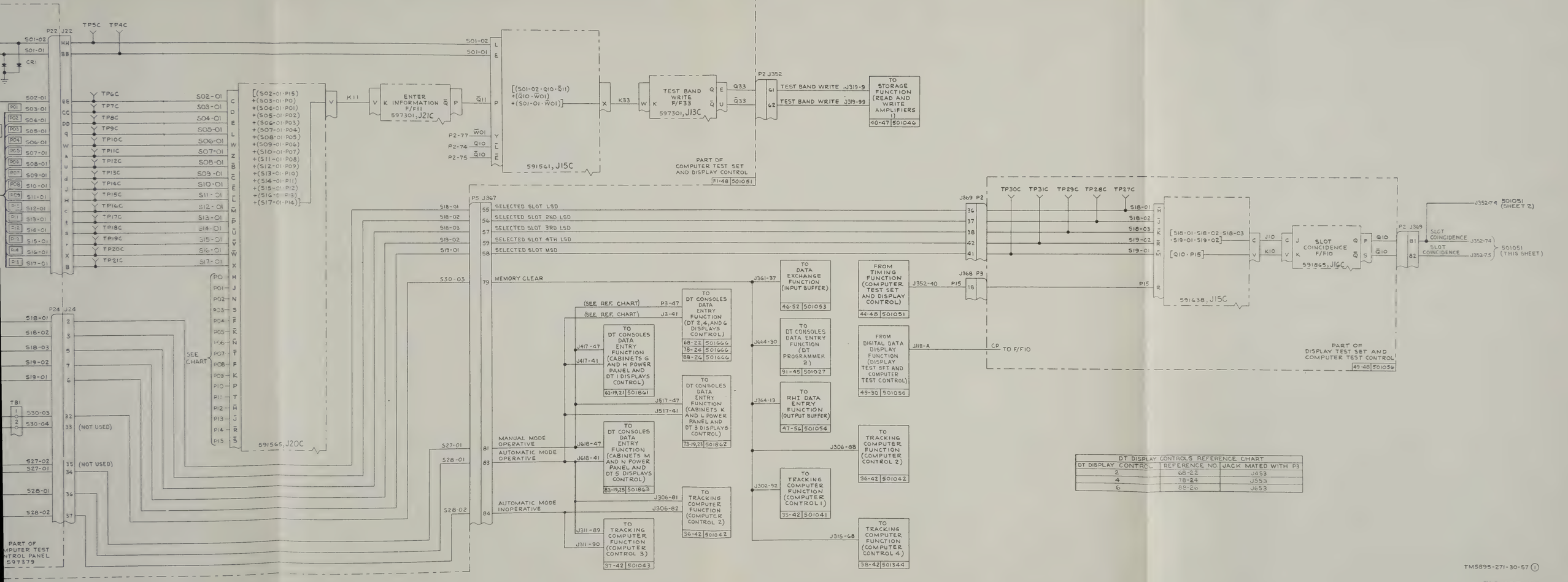
FIGURE 22



FROM TIMING FUNCTION (COMPUTER TEST SET AND DISPLAY CONTROL 501051)

SIGNAL	ORIGIN	TEST POINT	SHEET 1	SHEET 2
P00	J6C-H	TP15B	J20C-H	P22-AA, J15C-H
P01	J6C-U	TP16B	J20C-U	P22-GG
P02	J6C-N	TP17B	J20C-N	P22-FF
P03	J6C-S	TP18B	J20C-S	P22-n
P04	J6C-F̄	TP19B	J20C-F	P22-U
P05	J6C-K̄	TP20B	J20C-K	P22-w
P06	J6C-N̄	TP21B	J20C-N	P22-F
P07	J6C-T̄	TP22B	J20C-T	P22-K
P08	J6C-F	TP23B	J20C-F	P22-L
P09	J6C-K	TP24B	J20C-K	P22-g
P10	J6C-P	TP25B	J20C-P	
P11	J6C-T	TP26B	J20C-T	
P12	J6C-H̄	TP27B	J20C-H	
P13	J6C-J	TP28B	J20C-J	
P14	J6C-R̄	TP29B	J15C-R̄, J18C-R̄, J20C-R̄	
P15	J6C-S̄	TP30B	J20C-S̄	

Figure 22. Tracking computer test, detailed functional block diagram (part 1



DT DISPLAY CONTROLS REFERENCE CHART		
DT DISPLAY CONTROL	REFERENCE NO.	JACK MATED WITH P3
2	68-22	J453
4	78-24	J553
6	88-26	J653

Figure 22. Tracking computer test, detailed functional block diagram (part 1 of 3).

TM5895-271-30-57 (1)

FIGURE 22

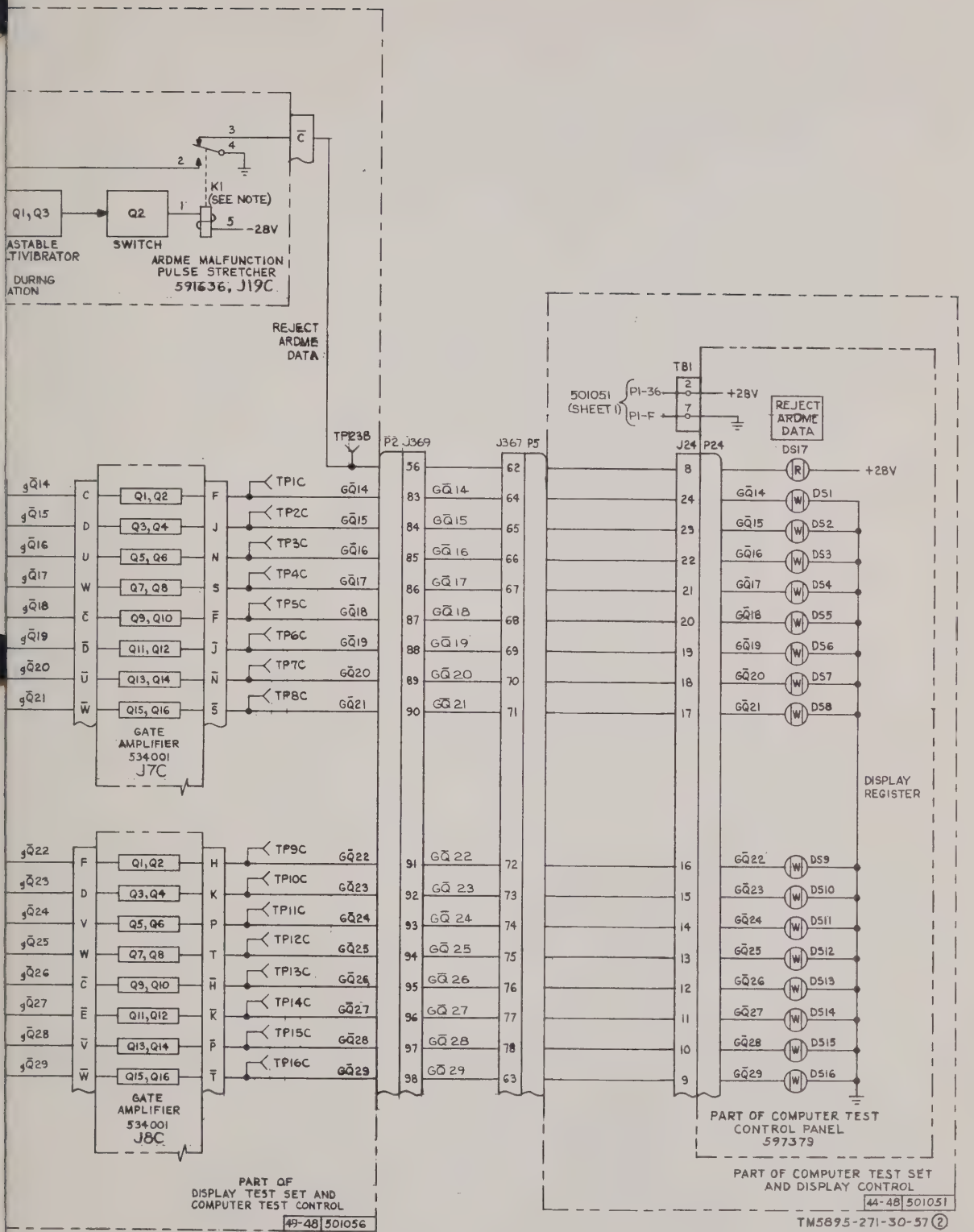

Q1, Q3
Q2
ASTABLE
TIVIBRATOR
SWITCH
DURING
ATION
K1
(SEE NOTE)
-28V
ARDME MALFUNCTION
PULSE STRETCHER
591636, J19C
REJECT
ARDME
DATA
TP238
P2 J369
J367 P5
TB1
501051
(SHEET 1)
P1-36
P1-F
+28V
REJECT
ARDME
DATA
J24 P24
DS17
GATE
AMPLIFIER
534001
J7C
GATE
AMPLIFIER
534001
J8C
DISPLAY
REGISTER
PART OF COMPUTER TEST
CONTROL PANEL
597379
PART OF COMPUTER TEST SET
AND DISPLAY CONTROL
44-48 501051
PART OF
DISPLAY TEST SET AND
COMPUTER TEST CONTROL
49-48 501056
TM5895-271-30-57 (2)

FIGURE 22

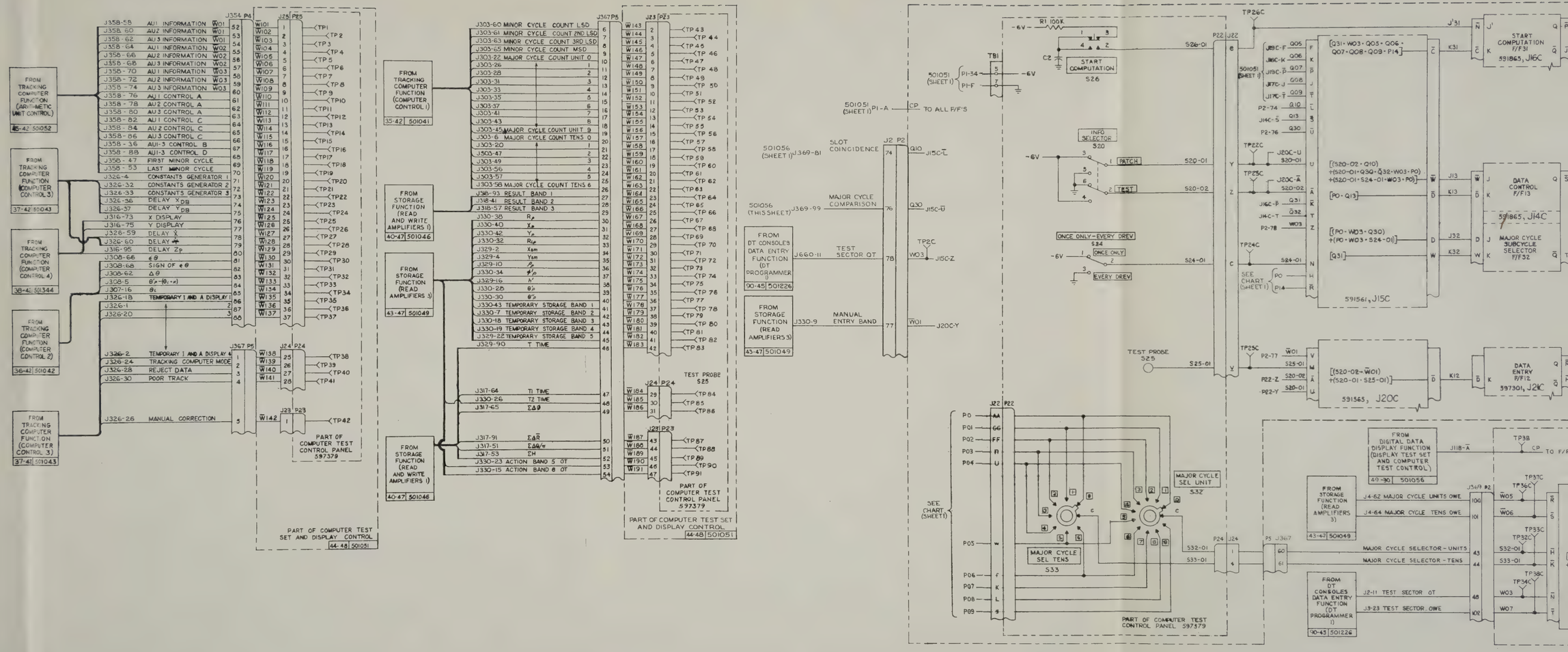
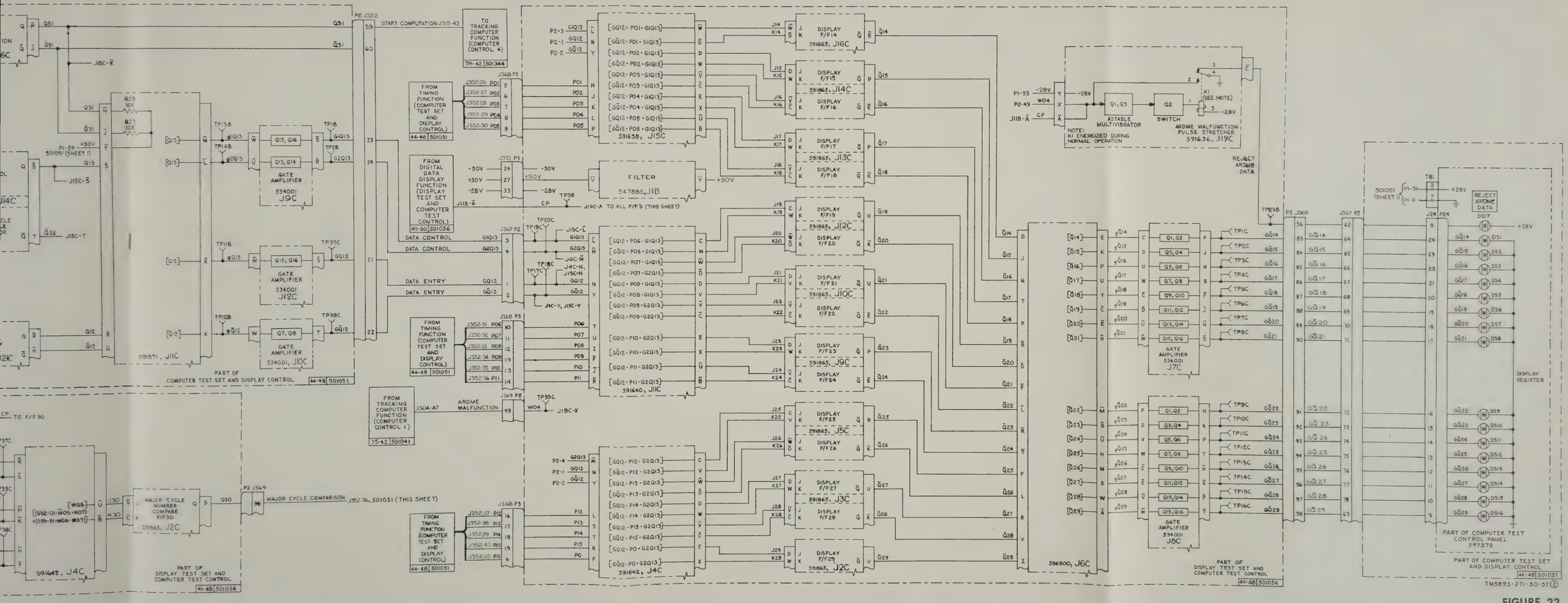


Figure 22. Tracking com



king computer test, detailed functional block diagram (part 2 of 3).

FIGURE 22

TEST BAND SLOT COUNTER OUTPUT SIGNALS

GNAL AME	ORIGIN	DESTINATION									
		TRACKING COMPUTER FUNCTION								ARDME FUNCTION	
		COMPUTER CONTROL 1		COMPUTER CONTROL 2		COMPUTER CONTROL 3		COMPUTER CONTROL 4		ARDME CONTROL 2	
	501051 UNIT	35-41	501041	36-42	501042	37-42	501043	38-42	501344	19-41	501123
	PIN NUMBER	PIN NUMBER		PIN NUMBER		PIN NUMBER		PIN NUMBER		PIN NUMBER	
LSD	J352-63					J311-92					
LSD	J352-64					J311-93					
LSD	J352-65			J306-89				J315-75			
LSD	J352-66	J302-31		J306-91						J211-99	
LSD	J352-67	J302-15		J306-90							
LSD	J352-68							J315-76		J211-33	
ND LSD	J352-69					J311-94					
D LSD	J352-70			J306-93				J315-77			
D LSD	J352-71	J302-46		J306-94						J211-98	
D LSD	J352-72					J311-95					
D LSD	J352-3			J306-96		J311-96					
D LSD	J352-6					J311-97					
D LSD	J352-7			J306-97				J315-80			
D LSD	J352-8	J302-47								J211-96	
H LSD	J352-9					J311-98					
H LSD	J352-10							J315-81			
H LSD	J352-11	J302-18		J306-100						J211-87	
H LSD	J352-12					J311-99					
SD	J352-15					J311-100					
SD	J352-16							J315-83		J211-73	
SD	J352-17	J302-90		J306-102							
SD	J352-18					J311-101					
SD	J352-19			J306-101						J211-45	
SD	J352-20	J302-19						J315-85			
	501056 UNIT										
D LSD	J369-58							J315-78		J211-46	
D LSD	J369-60	J302-16		J306-95							
D LSD	J369-57							J315-79			
D LSD	J369-61	J302-17		J306-98						J211-61	
H LSD	J369-62	J302-48								J211-85	
H LSD	J369-59			J306-99				J315-82			

TM5895-271-30-57③

FIGURE 22

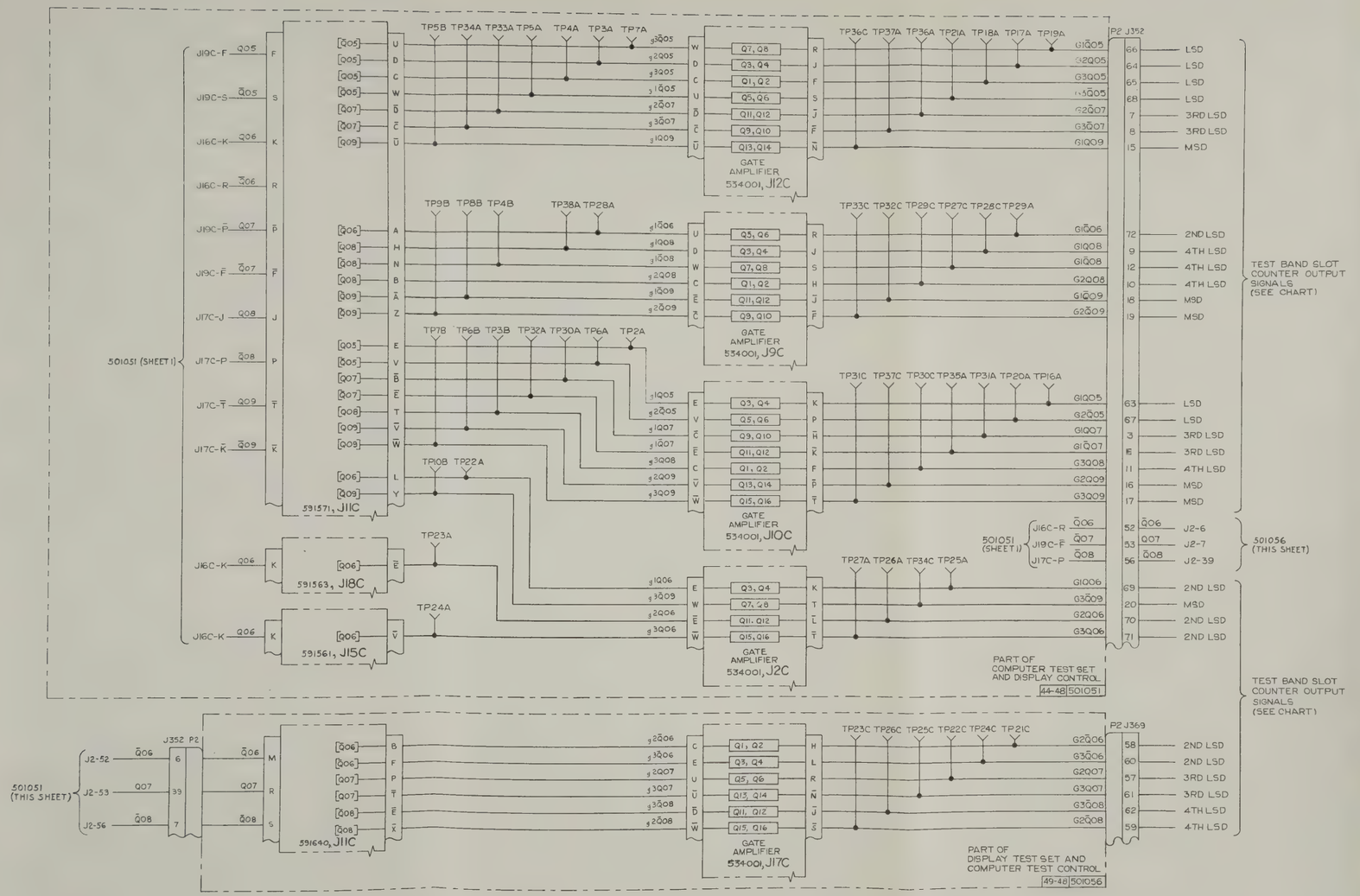


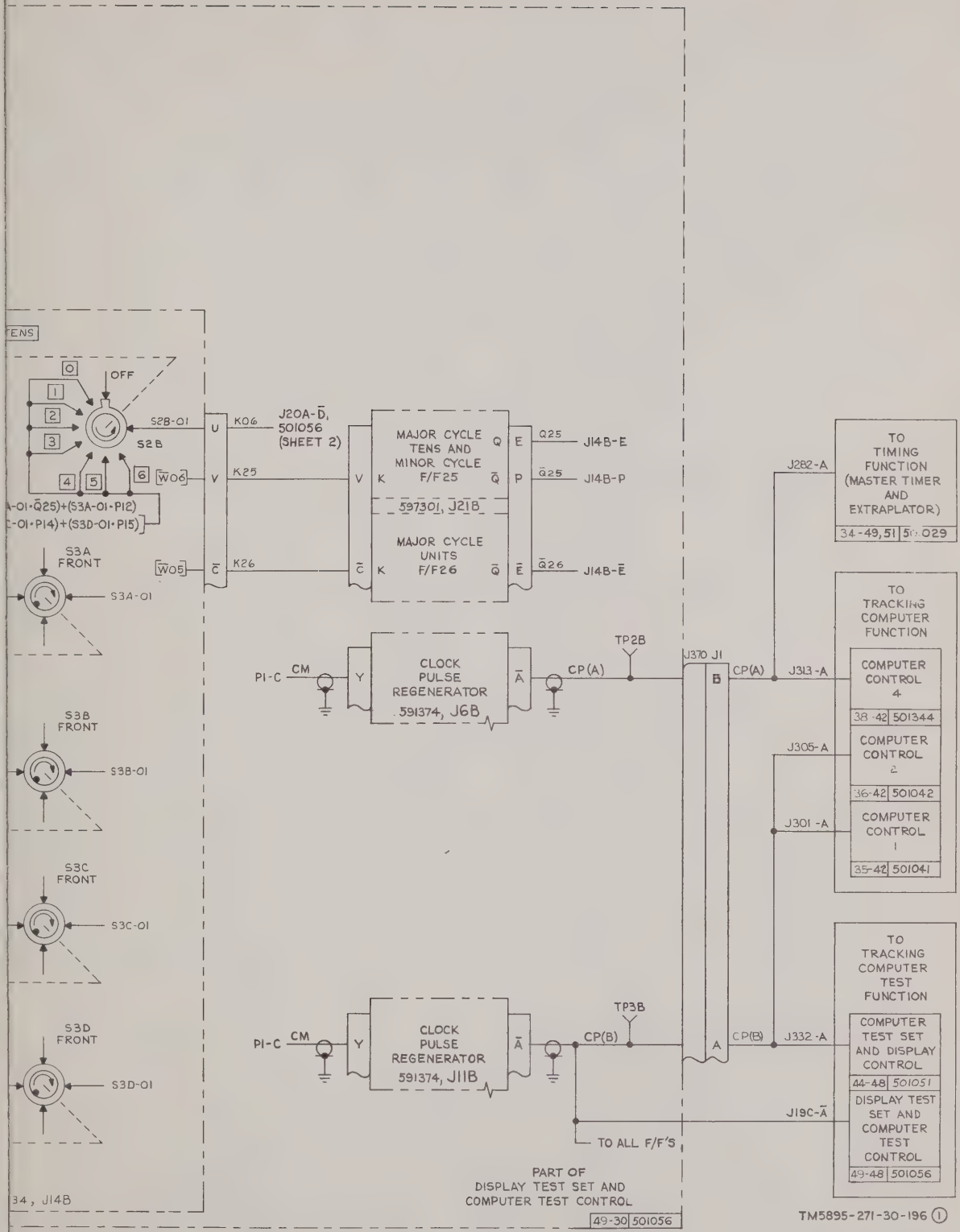
Figure 22. Tracking computer test, detailed functional block diagram (part 3 of 3).

TEST BAND SLOT COUNTER OUTPUT SIGNALS

SIGNAL NAME	ORIGIN	DESTINATION									
		TRACKING COMPUTER FUNCTION								ARDME FUNCTION	
		COMPUTER CONTROL 1		COMPUTER CONTROL 2		COMPUTER CONTROL 3		COMPUTER CONTROL 4		ARDME CONTROL 2	
	501051 UNIT	35-41	501041	36-42	501042	37-42	501043	38-42	501344	19-41	501123
	PIN NUMBER	PIN NUMBER		PIN NUMBER		PIN NUMBER		PIN NUMBER		PIN NUMBER	
LSD	J352-63					J311-92					
LSD	J352-64					J311-93					
LSD	J352-65			J306-89				J315-75			
LSD	J352-66	J302-31		J306-91						J211-99	
LSD	J352-67	J302-15		J306-90							
LSD	J352-68							J315-76		J211-33	
2ND LSD	J352-69					J311-94					
2ND LSD	J352-70			J306-93				J315-77			
2ND LSD	J352-71	J302-46		J306-94						J211-98	
2ND LSD	J352-72					J311-95					
3RD LSD	J352-3			J306-96		J311-96					
3RD LSD	J352-6					J311-97					
3RD LSD	J352-7			J306-97				J315-80			
3RD LSD	J352-8	J302-47								J211-96	
4TH LSD	J352-9					J311-98					
4TH LSD	J352-10							J315-81			
4TH LSD	J352-11	J302-18		J306-100						J211-87	
4TH LSD	J352-12					J311-99					
MSD	J352-15					J311-100					
MSD	J352-16							J315-83		J211-73	
MSD	J352-17	J302-90		J306-102							
MSD	J352-18					J311-101					
MSD	J352-19			J306-101						J211-45	
MSD	J352-20	J302-19						J315-85			
	501056 UNIT										
2ND LSD	J369-58							J315-78		J211-46	
2ND LSD	J369-60	J302-16		J306-95							
3RD LSD	J369-57							J315-79			
3RD LSD	J369-61	J302-17		J306-98						J211-61	
4TH LSD	J369-62	J302-48								J211-85	
4TH LSD	J369-59			J306-99				J315-82			

TM5895-271-30-57③

FIGURE 22



TM5895-271-30-196 (1)

FIGURE 23

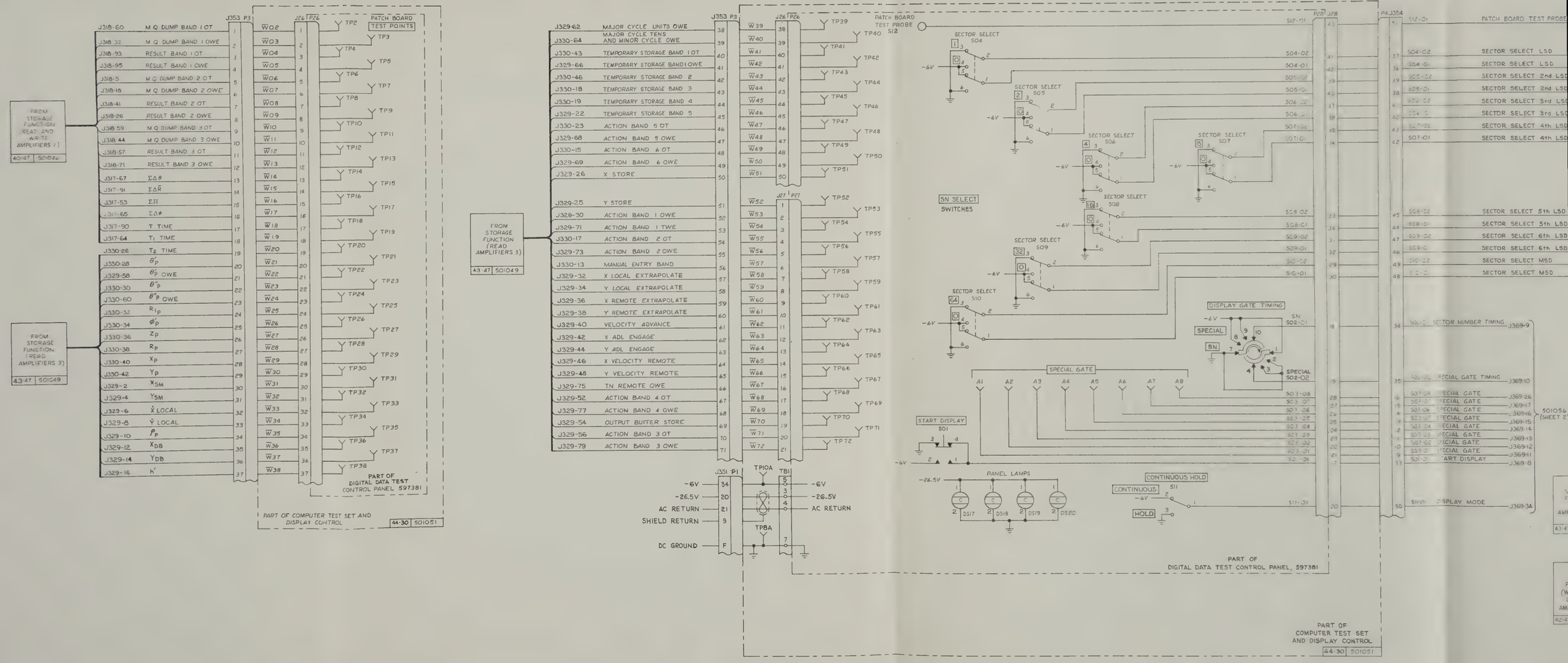
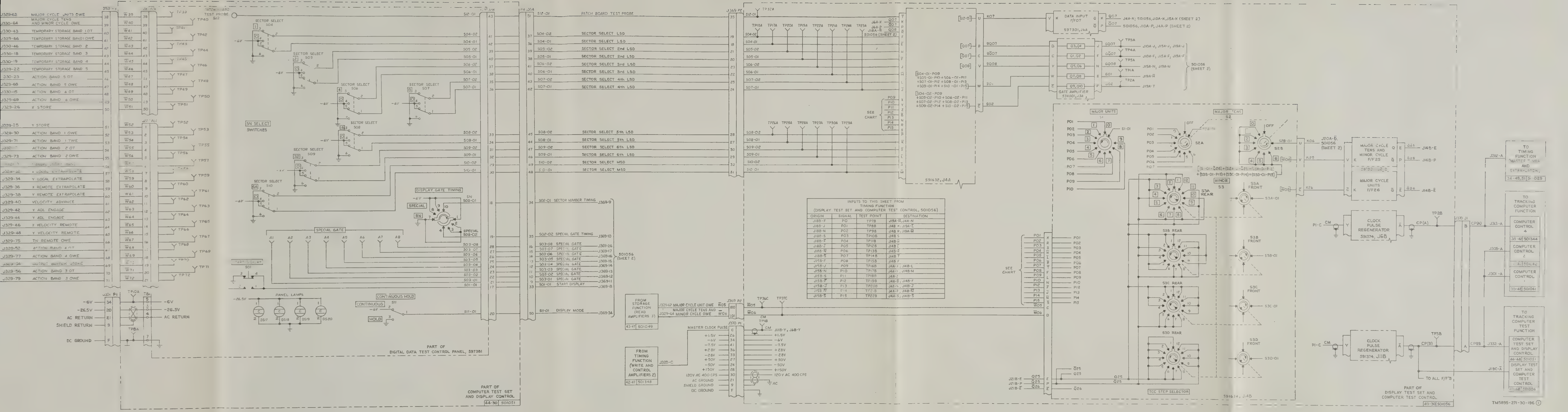

FROM STORAGE FUNCTION (READ AND WRITE AMPLIFIERS 1)
40-47 | 501046
FROM STORAGE FUNCTION (READ AMPLIFIERS 3)
43-47 | 501049
FROM STORAGE FUNCTION (READ AMPLIFIERS 3)
43-47 | 501049
J318-60 M Q DUMP BAND 1 OT
J318-32 M Q DUMP BAND 1 OWE
J318-93 RESULT BAND 1 OT
J318-95 RESULT BAND 1 OWE
J318-5 M Q DUMP BAND 2 OT
J318-18 M Q DUMP BAND 2 OWE
J318-41 RESULT BAND 2 OT
J318-26 RESULT BAND 2 OWE
J318-59 M Q DUMP BAND 3 OT
J318-44 M Q DUMP BAND 3 OWE
J318-57 RESULT BAND 3 OT
J318-71 RESULT BAND 3 OWE
J317-67 ΣΔθ
J317-91 ΣΔR̄
J317-53 ΣH
J317-65 ΣΔΦ
J317-90 T TIME
J317-64 T1 TIME
J330-26 T2 TIME
J330-28 θ̄p
J329-58 θ̄p OWE
J330-30 θ̄̄p
J330-60 θ̄̄p OWE
J330-32 R1p
J330-34 Φ̄p
J330-36 Zp
J330-38 Rp
J330-40 Xp
J330-42 Yp
J329-2 XSM
J329-4 YSM
J329-6 X̄ LOCAL
J329-8 Ȳ LOCAL
J329-10 P̄p
J329-12 XDB
J329-14 YDB
J329-16 h̄'
J353 P3
J26 P26
W̄02 W̄03 W̄04 W̄05 W̄06 W̄07 W̄08 W̄09 W̄10 W̄11 W̄12 W̄13 W̄14 W̄15 W̄16 W̄17 W̄18 W̄19 W̄20 W̄21 W̄22 W̄23 W̄24 W̄25 W̄26 W̄27 W̄28 W̄29 W̄30 W̄31 W̄32 W̄33 W̄34 W̄35 W̄36 W̄37 W̄38
PATCH BOARD TEST POINTS
TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24 TP25 TP26 TP27 TP28 TP29 TP30 TP31 TP32 TP33 TP34 TP35 TP36 TP37 TP38
PART OF DIGITAL DATA TEST CONTROL PANEL 597381
PART OF COMPUTER TEST SET AND DISPLAY CONTROL
44-30 | 501051
J329-62 MAJOR CYCLE UNITS OWE
J330-64 MAJOR CYCLE TENS AND MINOR CYCLE OWE
J330-43 TEMPORARY STORAGE BAND 1 OT
J329-66 TEMPORARY STORAGE BAND1 OWE
J330-46 TEMPORARY STORAGE BAND 2
J330-18 TEMPORARY STORAGE BAND 3
J330-19 TEMPORARY STORAGE BAND 4
J329-22 TEMPORARY STORAGE BAND 5
J330-23 ACTION BAND 5 OT
J329-68 ACTION BAND 5 OWE
J330-15 ACTION BAND 6 OT
J329-69 ACTION BAND 6 OWE
J329-26 X STORE
J329-25 Y STORE
J329-30 ACTION BAND 1 OWE
J329-71 ACTION BAND 1 TWE
J330-17 ACTION BAND 2 OT
J329-73 ACTION BAND 2 OWE
J330-13 MANUAL ENTRY BAND
J329-32 X LOCAL EXTRAPOLATE
J329-34 Y LOCAL EXTRAPOLATE
J329-36 X REMOTE EXTRAPOLATE
J329-38 Y REMOTE EXTRAPOLATE
J329-40 VELOCITY ADVANCE
J329-42 X ADL ENGAGE
J329-44 Y ADL ENGAGE
J329-46 X VELOCITY REMOTE
J329-48 Y VELOCITY REMOTE
J329-75 TN REMOTE OWE
J329-52 ACTION BAND 4 OT
J329-77 ACTION BAND 4 OWE
J329-54 OUTPUT BUFFER STORE
J329-56 ACTION BAND 3 OT
J329-79 ACTION BAND 3 OWE
J353 P3
J26 P26
W̄39 W̄40 W̄41 W̄42 W̄43 W̄44 W̄45 W̄46 W̄47 W̄48 W̄49 W̄50 W̄51
TP39 TP40 TP41 TP42 TP43 TP44 TP45 TP46 TP47 TP48 TP49 TP50 TP51
J27 P27
W̄52 W̄53 W̄54 W̄55 W̄56 W̄57 W̄58 W̄59 W̄60 W̄61 W̄62 W̄63 W̄64 W̄65 W̄66 W̄67 W̄68 W̄69 W̄70 W̄71 W̄72
TP52 TP53 TP54 TP55 TP56 TP57 TP58 TP59 TP60 TP61 TP62 TP63 TP64 TP65 TP66 TP67 TP68 TP69 TP70 TP71 TP72
J351 P1
TP10A
TB11
-6V 34 5 -6V
-26.5V 20 3 -26.5V
AC RETURN 21 4 AC RETURN
SHIELD RETURN 9
TP8A
DC GROUND F 7
PATCH BOARD TEST PROBE S12
SECTOR SELECT S04
SECTOR SELECT S05
SECTOR SELECT S06
SECTOR SELECT S07
SECTOR SELECT S08
SECTOR SELECT S09
SECTOR SELECT S10
SN SELECT SWITCHES
DISPLAY GATE TIMING
SPECIAL
SN
SPECIAL S02-02
SN S02-01
SPECIAL GATE
A1 A2 A3 A4 A5 A6 A7 A8
START DISPLAY S01
PANEL LAMPS
-26.5V
DS17 DS18 DS19 DS20
CONTINUOUS HOLD
CONTINUOUS S11
HOLD
S12-01
S04-02
S04-01
S05-02
S05-01
S06-02
S06-01
S07-02
S07-01
S08-02
S08-01
S09-02
S09-01
S10-02
S10-01
S03-08
S03-07
S03-06
S03-05
S03-04
S03-03
S03-02
S03-01
S02-01
S11-01
P28 J28
P4 J354
S12-01 PATCH BOARD TEST PROBE
S04-02 SECTOR SELECT LSD
S04-01 SECTOR SELECT LSD
S05-02 SECTOR SELECT 2nd LSD
S05-01 SECTOR SELECT 2nd LSD
S06-02 SECTOR SELECT 3rd LSD
S06-01 SECTOR SELECT 3rd LSD
S07-02 SECTOR SELECT 4th LSD
S07-01 SECTOR SELECT 4th LSD
S08-02 SECTOR SELECT 5th LSD
S08-01 SECTOR SELECT 5th LSD
S09-02 SECTOR SELECT 6th LSD
S09-01 SECTOR SELECT 6th LSD
S10-02 SECTOR SELECT MSD
S10-01 SECTOR SELECT MSD
S02-02 SECTOR NUMBER TIMING J369-9
S02-01 SPECIAL GATE TIMING J369-10
S03-08 SPECIAL GATE J369-26
S03-07 SPECIAL GATE J369-17
S03-06 SPECIAL GATE J369-16
S03-05 SPECIAL GATE J369-15
S03-04 SPECIAL GATE J369-14
S03-03 SPECIAL GATE J369-13
S03-02 SPECIAL GATE J369-12
S03-01 SPECIAL GATE J369-11
S01-01 ART DISPLAY J369-8
S11-01 DISPLAY MODE J369-34
501056 (SHEET 2)
PART OF DIGITAL DATA TEST CONTROL PANEL, 597381
PART OF COMPUTER TEST SET AND DISPLAY CONTROL
44-30 | 501051

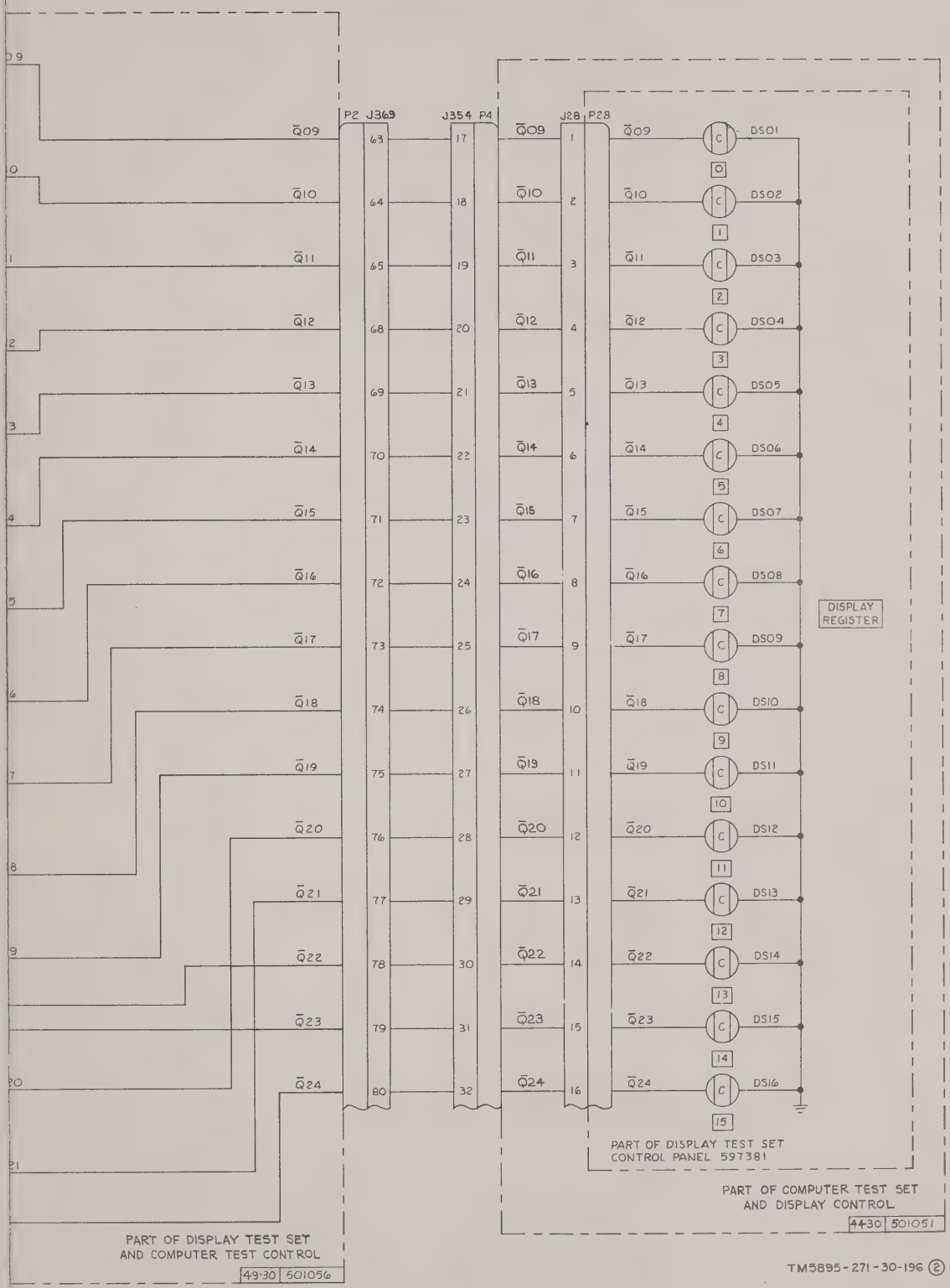
Figure 23.



INPUTS TO THIS SHEET FROM TIMING FUNCTION (DISPLAY TEST SET AND COMPUTER TEST CONTROL, 501056)			
ORIGIN	SIGNAL	TEST POINT	DESTINATION
J18B-F	P0	TP7B	J19A-$\overline{N}$, J4A-N
J18B-J	P01	TP8B	J14B K; J19A-$\overline{L}$
J18B-N	P02	TP9B	J14B R; J19A-$\overline{M}$
J18B-S	P03	TP10B	J14B S
J18B-$\overline{F}$	P04	TP11B	J14B-$\overline{H}$
J18B-$\overline{J}$	P05	TP12B	J14B $\overline{L}$
J18B-$\overline{N}$	P06	TP13B	J14B-$\overline{R}$
J18B-$\overline{S}$	P07	TP14B	J14B $\overline{T}$
J15B-F	P08	TP15B	J14B F
J15B-J	P09	TP16B	J4A-X ; J14B-L
J15B-N	P10	TP17B	J4A-Y , J14B-N
J15B-S	P11	TP18B	J4A-Z
J15B-$\overline{F}$	P12	TP19B	J4A-$\overline{B}$; J14B-F
J15B-$\overline{J}$	P13	TP20B	J4A-W , J14B-$\overline{J}$
J15B $\overline{N}$	P14	TP21B	J4A-R , J14B-$\overline{N}$
J15B-$\overline{S}$	P15	TP22B	J4A-S ; J14B-$\overline{S}$

Figure 23. Digital data display, detailed functional block diagram (part 1 of 2).

FIGURE 23



TM5895-271-30-196 (2)

FIGURE 23

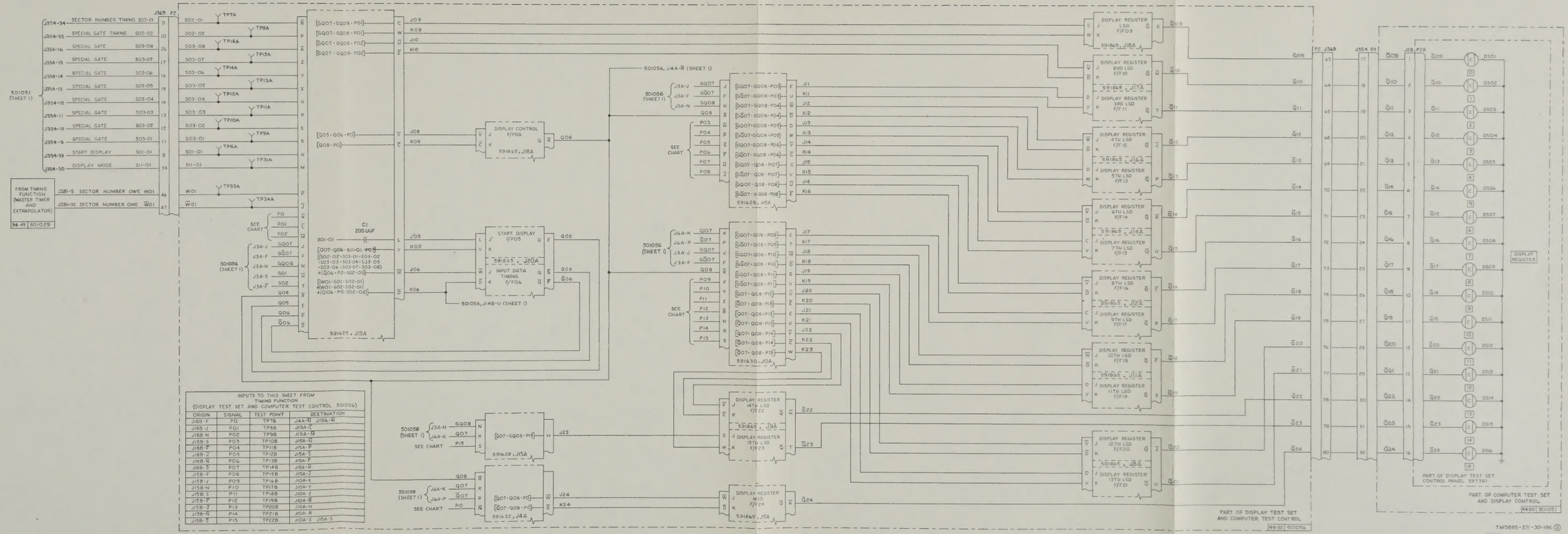


Figure 23. Digital data display, detailed functional block diagram (part 2 of 2).

FIGURE 23